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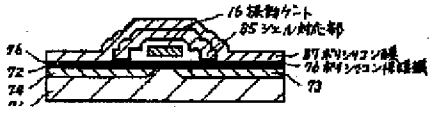
(54) OSCILLATORY TRANSDUCER AND FABRICATION THEREOF

(57) Abstract:

PROBLEM TO BE SOLVED: To prevent adhesion of an oscillatory gate by covering a gate oxide with polysilicon and providing a planar conductive oscillatory gate which is displaced by an electrostatic power generated with respect to a drain through self-oscillation thereby protecting a gate insulator and preventing drift.

SOLUTION: A gate oxide 72 is deposited on a substrate 71 and a stable polysilicon protective layer 76 resistant to hydrofluoric acid is formed thereon. A first sacrificial layer oxide film is then deposited on the polysilicon protective layer 76 and a polysilicon is deposited thereon and doped with boron. Subsequently, the polysilicon is etched into a predetermined shape and an oscillatory gate 16, i.e., a planar beam, is formed. Finally, a second sacrifice oxide is deposited on the first sacrifice oxide.



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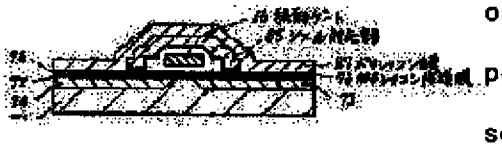

(57)Abstract:

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SOLUTION: A gate oxide 72 is deposited on a substrate 71 and a stable polysilicon protective layer 76 resistant to hydrofluoric acid is formed thereon. A first sacrificial layer oxide film is then deposited on the polysilicon protective layer 76 and a polysilicon is deposited thereon and doped with boron. Subsequently, the polysilicon is etched into a predetermined shape and an oscillatory gate 16, i.e., a planar beam, is formed. Finally, a second sacrifice oxide is deposited on the first sacrifice oxide.

CLAIMS

[Claim(s)]

[Claim 1]An oscillating-type transducer comprising:

A substrate of a semiconductor which has the 1st conduction type type in an oscillating-type transducer which measures distortion added to both ends of this vibration gate when both ends measured resonance frequency of a vibration gate fixed to

a substrate.

A drain which is formed in the surface of this substrate and has the 2nd conduction type type contrary to said conduction type type, and a channel inserted with sauce.

Gate oxide formed on the surface of said substrate.

This gate oxide top A wrap polysilicon protective film, A tabular conductive vibration gate displaced according to electrostatic force which it is fixed to said substrate, and both ends cover said drain, sauce, and a channel, are arranged [holds a gap from the surface of this polysilicon protective film, and], and is produced between these drains by self-oscillation so that it may consist of polysilicon and can be displaced.

[Claim 2]The oscillating-type transducer according to claim 1, wherein at least one place possesses a polysilicon protective film electrically connected to said semiconductor substrate or said vibration gate.

[Claim 3]The oscillating-type transducer possessing a conduction part formed in a portion of said polysilicon protective film which counters said channel by spreading an impurity according to claim 1 or 2.

[Claim 4]The oscillating-type transducer possessing SHIERU by which an inside of a cover was held in said vibration gate at a vacuum according to claim 1, 2, or 3.

[Claim 5]A manufacturing method of an oscillating-type transducer having the following processes in a manufacturing method of an oscillating-type transducer which measures distortion added to both ends of this vibration gate when both ends measured resonance frequency of a vibration gate fixed to a substrate.

(a) A gate oxide formation process which forms gate oxide on a substrate of a semiconductor which has the 1st conduction type type.

(b) An ion implantation process which carries out the ion implantation of the impurity used as the 2nd conduction type type to a predetermined region corresponding to sauce, a drain, or a lead part of a gate.

(c) A polysilicon protection film formation process which forms a polysilicon protective film on said gate oxide.

(d) The 1st sacrifice layer oxide film formation process which forms the 1st sacrifice

layer oxide film on this polysilicon protective film.

(e) Form a polysilicon film on this 1st sacrifice layer oxide film. Then, an impurity which serves as the 2nd conduction type type for addition of conductivity is doped. A beam building process of etching this polysilicon film and forming a beam corresponding to a vibration gate.

(f) The 2nd sacrifice layer oxide film formation process which forms the 2nd sacrifice layer oxide film on said 1st sacrifice layer oxide film and said beam.

(g) A gap corresponding point formation process which etches said 1st and 2nd sacrifice layer oxide film, and forms a gap corresponding point.

(h) A film formation process corresponding to a gap which forms an oxide film corresponding to a gap as a sacrifice layer in the whole surface including a said polysilicon protective film and gap corresponding point top.

(i) Form a polysilicon film on an oxide film corresponding to this gap. A shell corresponding point formation process which etches this polysilicon film and forms a shell corresponding point.

(j) An etching gap formation process of etching an oxide film corresponding to said gap, forming an introducing hole, and also removing said gap corresponding point via this introducing hole.

(k) A vacuum lock process of forming said said shell corresponding point, said introducing hole, and polysilicon protective film top with a polysilicon film, and holding an inside of shell to a vacuum in a vacuum.

(l) Carry out etching removal of some of said gate oxides in the upper part of said source part and said drain part, said polysilicon protective films, and said polysilicon films, carry out an opening, and form a contact hole. Then, an electrode formation process which forms a pad portion in this contact hole part, and wires by carrying out bonding by a gold streak.

(m) A diaphragm formation process which etches a pars basilaris ossis occipitalis of a substrate of a semiconductor which has said 1st conduction type type, and forms a diaphragm.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]Gate dielectric film is protected, and this invention can prevent a drift, and relates to the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method.

[0002]

[Description of the Prior Art]Drawing 16 is a theoretic composition explanatory view of the conventional example currently generally used conventionally, is the example using the oscillating-type transducer as a pressure sensor, and is shown in JP,7-30128,A, for example.

[0003]As for the silicon substrate 1, for example, a conduction type type is formed in n form, the electrode 2 is fixed here, and the electrode 2 is connected to common potential point COM. The impurity of p form is spread on the upper surface of this silicon substrate 1, the sauce S is formed in it, and the electrode 3 for taking out the potential of the sauce S here is formed in it. Pressure P_M which should be measured is impressed to the undersurface of this silicon substrate 1.

[0004]Only the prescribed interval W is left to this sauce S, similarly the impurity of p form is spread on the upper surface of the silicon substrate 1, the drain D is formed, and the electrode 4 for taking out the potential of the drain D is formed here.

[0005]Only x_1 is left above the portion of the prescribed interval W of the silicon substrate 1, the heights 5 and 6 are formed in it, and the both ends of the vibration gate 7 (the numerals which G become expedient may be used) which functions as a tabular vibrator to which the impurity was spread and conductivity was given are being fixed to the heights 5 and 6, such as this.

[0006]That is, although only x_1 is left and arranged except for both ends and the vibration gate 7 and the silicon substrate 1 are not illustrated by the silicon substrate 1 corresponding to this vibration gate 7, channel CNN1 is formed between the drain D and

the sauce S.

[0007]Between the electrode 4 and common potential point COM, the resistance R1 and DC power supply E1 are connected in series, and the potential of the drain D is held to common potential point COM at negative potential. It is connected to the vibration gate 7 so that DC power supply E2 may become negative potential to common potential point COM.

[0008]Drawing 17 is an explanatory view explaining operation of drawing 16. It has composition including the section of the silicon substrate 1 seen from the longitudinal direction of the vibration gate 7. Since electronegative potential is impressed to the vibration gate 7 which functions as a gate from DC power supply E2, as shown in drawing 17, it is pushed aside by the electron inside the silicon substrate 1 (drawing 17 Shimo) from the surface of Shimo of the vibrator 7, and an electron hole can be conversely drawn near to the surface.

[0009]Channel CNN1 which is a conduction layer of thin P type will be formed in the surface of the electron hole (P type) which was able to be drawn near, between the drains D (P type) will be connected with P type to the sauce S (P type), and, for this reason, current i_{d1} flows between the sauce S and the drain D.

[0010]The voltage of the drain D generated by this current i_{d1}, The electrostatic suction force between the vibration gate 7 and the drain D is changed by the electrical change which received the phase shift and received this phase shift by drain resistance R_D and electric capacity C_D formed between a drain and the silicon substrate 1, and interval x_1 is changed.

[0011]The thickness of channel CNN1 is changed by change of this interval x_1, current i_{d1} is changed by this, and this causes the electrical change of a drain. Although this is repeated and it oscillates, this oscillation is continued by selecting so that the product (omegaR_DC_D) of drain resistance R_D, the drain D and electric capacity C_D between the silicon substrates 1, and oscillation angular velocity omega of an oscillation may become very large compared with 1.

[0012]In the state where self-oscillation is maintained as mentioned above, if pressure P_M is impressed to the silicon substrate 1 like a graphic display, distortion by this

pressure P_M will be added to the vibration gate 7 via the heights 5 and 6 which fix the vibration gate 7, and character frequency will change corresponding to this. Therefore, the value of pressure P_M is detectable by taking out change of this character frequency.

[0013]The perspective view and drawing 19 which drawing 18 shows the composition of the concrete example of drawing 16 are a sectional view near [the] the center section. However, the vibration gate is omitted about wrap shell portions and a diaphragm portion. Drawing 20 is a whole sectional side elevation in the center portion of a vibration gate.

[0014]In drawing 18, drawing 19, and drawing 20, the silicon substrate 11, For example, a conduction type type is formed in n form, the impurity of p form is spread on the upper surface of this silicon substrate 11, the sauce S is formed in it, and the electrode 12 made from aluminum for taking out the potential of the sauce S is formed here via wiring section W_S shown by a dotted line. Although not illustrated in the undersurface of this silicon substrate 11, pressure P_M which a diaphragm is formed in recessed shape and should measure here is impressed.

[0015]Only a prescribed interval is left to this sauce S, similarly the impurity of p form is spread on the upper surface of the silicon substrate 11, the drain D is formed, and the electrode 13 made from aluminum for taking out the potential of the drain D is formed here via wiring section W_D shown by a dotted line.

[0016]Only gap x_2 is left above the silicon substrate 11, the fixed ends 14 and 15 are formed in it, and the both ends of the tabular vibration gate 16 of the polysilicon in which the impurity was spread and conductivity was given are being fixed to the fixed ends 14 and 15, such as this, by one. The length of the beam of the vibration gate 16 is L. And this vibration gate 16 is connected via wiring part W_G shown by the electrode 17 and dotted line made from aluminum.

[0017]That is, except for both ends, the vibration gate 16 and the silicon substrate 11 leave only gap x_2, and are arranged, and channel CNN2 is formed between the drain D of the silicon substrate 11 and the sauce S corresponding to this vibration gate 16.

[0018]These drain [that were formed in the upper surface of the silicon substrate 11] D, and channel CNN2, and the corrosion-resistant high protective film [as opposed to hydrofluoric acid (HF) in the sauce S top] 18, for example, Si_3N_4, The two-layer structure

film 21 which consists of $S_iC_xN_y$, S_iC, AL_2O_3, etc. and the oxide film 19 is formed. The protective film 18 is the same insulator as the oxide film 19.

[0019]And between this two-layer structure film 21 and vibration gate 16, the gap is provided so that the vibration gate 16 can vibrate up and down considering the fixed ends 14 and 15 as a paragraph. Thus, the oscillating gauge 22 is constituted. 23 is SHIERU and 24 is a diaphragm.

[0020]The point which combines an oscillating gauge and an electronic circuit as shown in drawing 18, and constitutes an oscillating-type transducer from old explanation was explained. Next, the manufacturing method which manufactures the oscillating gauge 22 as a component of such an oscillating-type transducer is explained using the manufacturing process figure shown in drawing 21 and drawing 22.

[0021]Although the manufacturing process shown in drawing 22 continues succeeding the manufacturing process shown in drawing 21, it is divided into two on [of explanation] expedient. In the composition shown in drawing 18, since the section structures produced in process of a manufacturing process in the portion of the vibration gate 16 and the portion of the fixed ends 14 and 15 which fix this at both ends differ, although it is the same process, it separates into right and left and these are illustrated according to each.

[0022]In the section structure of the center section of the vibration gate 16, the right-hand side figure of the chart on the left is the section structure of the portion of the fixed end 14. Since the portion of the fixed end 15 is the same structure as the portion of the fixed end 14, it is omitted.

[0023]Step 1 shows a gate oxide formation process. The gate oxide 31 is formed on the substrate 30 of the silicon single crystal of n form at a thickness of about 500 A, for example. In this process, the section structure in the center section and fixed end part of a vibration gate is formed identically. Then, it shifts to Step 2. Henceforth, each step is gone on according to a step number.

[0024]Step 2 shows an ion implantation process. Here, the ion implantation of the boron is carried out to a predetermined region as p type impurities. This sets prescribed interval W_N which is due to form channel CCN in the center section of the vibration gate,

and the source part 32 (it corresponds to W_S of drawing 18) and the drain part 33 (it corresponds to W_D of drawing 18) of p form are formed, In a fixed end part, the gate lead part 34 (it corresponds to W_G of drawing 18) of p form is formed.

[0025]Step 3 shows a channel formation process. Here, the ion implantation of the boron is carried out to the channel section 34 (CCN2) of prescribed interval W_N which is due to form channel CCN in the center section of the vibration gate in the shallow depth. Resistance between source drains is controllable by this to a predetermined value. In this case, it is changeless in a fixed end part.

[0026]Step 4 shows a nitride formation process. In this process, for the protection of the gate oxide 31 to the hydrofluoric acid (HF) used by a post process. As the strong insulator layer 35, tolerance forms an $S_iC_xN_y$ film on the gate oxide 31 by a thickness of about about 1000 A to hydrofluoric acid, for example.

[0027]Step 5 shows the 1st sacrifice layer oxide film formation process. This process forms the oxide film 36 on the insulator layer 35 by the CVD (ChemicalVapour Deposition) method at a thickness of about 5000 A as a sacrifice layer of the bottom for forming an opening in the circumference of the vibration gate 16 eventually first.

[0028]Next, to a fixed end part, the portions of the gate oxide 31 of the portion of the schedule in which the fixed end 14 is formed by photolithographic technique, the insulator layer 35, and the oxide film 36 are used as the opening 37, and an opening is carried out.

[0029]Step 6 shows polysilicon stage film formation. This process is a previous process for forming the vibration gate 16 and the fixed end 14 eventually. First, the polysilicon 38 is formed by a thickness of about 1 micrometer on the oxide film 36 and the opening 37. Then, boron is doped in order to give conductivity.

[0030]Next, after making a mask the portion corresponding to the vibration gate 16, and the portion corresponding to the opening 37 with photolithographic technique, The support 40 of a Y-globe type is formed in the tabular beam 39 which etches the polysilicon 38 into predetermined shape by RIE (Reactive Ion Etching), and serves as a vibration gate eventually, and the opening 37.

[0031]Step 7 shows the 2nd sacrifice layer oxide film formation process. This process

forms the oxide film 41 on the oxide film 36, the beam 39, and the support 40 with a CVD method at a thickness of about 5000 A as a sacrifice layer of the portion except the bottom for forming an opening in the circumference of the vibration gate 16 eventually.

[0032]Step 8 shows an oxide film etching process. First, after carrying out the mask of the portion remove the neighborhood of the beam 39 in the center section of the vibration gate, and excluding Y character center section 42 of the support 40 near the support 40 in a fixed end part with photolithographic technique, the oxide films 36 and 41 of these circumferences are etched with hydrofluoric acid, and the gap corresponding points 43 and 44 are formed.

[0033]Step 9 shows the stage film formation corresponding to a gap. This process forms in the whole surface the oxide film 45 as a sacrifice layer for introducing the etching reagent used by a post process with a CVD method including the insulator layer 35 and gap corresponding point 43 and 44 top by a thickness of about about 500 A. Then, the oxide film 45 on Y character center section 42 is etched and removed using photolithographic technique.

[0034]Step 10 shows a SHIERU corresponding point formation process. The polysilicon 46 is formed so that it may become a thickness of about 1 micrometer on the oxide film 45 etc. which were formed at Step 9. Then, short time heat treatment of the stress which remains in polysilicon of SHIERU and a vibration gate by RTA (Rapid Thermal Aneal) is carried out, it is removed, and these are prevented from changing.

[0035]Then, a mask is carried out using photolithographic technique, the polysilicon 46 is etched by RIE, and the SHIERU corresponding point 47 is formed in the range of a wrap size for a vibration gate.

[0036]Step 11 shows an etching gap formation process. In order to form a vibration gate and SHIERU, using hydrofluoric acid and etching the oxide film 45, this process removes this, forms the introducing hole 48 and, subsequently also removes the gap corresponding points 43 and 44 via this introducing hole 48. Thus, the vibration gate 16, the fixed end 14, and SHIERU 49 are formed.

[0037]Step 12 shows a vacuum lock process. This process forms the SHIERU 49, introducing hole 48, and insulator layer 35 top by a thickness of about about 5000 A with

the polysilicon 50 in a vacuum, and holds the inside of SHIERU 49 to a vacuum.

[0038]Step 13 shows a contact hole formation process. The opening of some of gate oxides 31 in the upper part of the source part 32 and the drain part 33, insulator layers 35, and polysilicon 50 is carried out using photolithographic technique and RIE, and the contact holes 51 and 52 are formed. Similarly, the contact hole 54 can be formed also in a gate section.

[0039]Step 14 shows a diaphragm formation process. The pars basilaris ossis occipitalis of the substrate 30 of a silicon single crystal is etched, and the diaphragm 53 is formed so that a center section may turn into a thin-walled part which becomes heavy-gage in the circumference with thin meat using potassium hydrate (KOH) liquid.

[0040]Step 15 shows a bonding process. The electrodes 13 and 12 made from aluminum are formed in the contact holes 51 and 52. The above is a manufacturing method which covers the oscillating gauge of an oscillating-type transducer by shell, and forms a diaphragm.

[0041]

[Problem(s) to be Solved by the Invention]However, there are the following problems in such a structural form transducer formed on the semiconductor substrate using ultra-fine processing technology (micromachining).

[0042]1) In order to use the silicon oxide 36 and 41 for a sacrifice layer at the process of producing structures, such as the vibration gate 16, it is necessary to etch with hydrofluoric acid at the process of removing this for a long time. Although it is necessary to protect the film which I do not want to provide in the silicon substrate 11 side and to etch the gate oxide 19 required as an insulator layer etc. at this time by the gate oxide 19 and the high protective film 18 of hydrofluoric acid-proof nature of the same silicon nitride film 18 grade that is an insulating material, Sufficient corrosion resistance was not acquired.

[0043]2) Furthermore, if the gate oxide 19 is protected by the high protective film of hydrofluoric acid-proof nature, such as a silicon nitrogen-ized film, since level is made to an interface with the gate oxide 19, by the film of silicon nitride film 18 grade, The absolute value of the threshold voltage of the portion equivalent to FET becomes large,

and and ********** and variation become large. Since the level of this interface is unstable, it causes degradation of electrical properties, such as a drift.

[0044]In this structure, since the electrode section equivalent to the gate of the usual MOSFET is not in contact with an insulator layer, a result which an electric potential gradient occurs, and the potential near the sauce falls horizontally in an insulator layer, therefore pushes up threshold voltage has been brought.

[0045]For this reason, when the operating point was fixed, the size of drain current had a problem out of which dispersion comes or which a drift produces.

3) There is a problem that the vibration gate 16 will adhere to the silicon substrate 11, working [in a manufacturing process or after completion], and rigid small beam structure was seldom able to be produced.

[0046]However, if it is going to acquire a big frequency change rate when it is going to produce the oscillating-type sensor of the high sensitivity which has beam structure, Although thickness must be made [length / of a beam] thin, since such a beam had small rigidity and it adhered to a silicon substrate easily for a long time, it was difficult to produce a high sensitivity oscillating-type sensor.

[0047]The following solutions were adopted to the above problems.

1) The corrosion resistance of a polysilicon film over hydrofluoric acid solution is strong enough as compared with silicon nitride film 18 grade, and although the silicon oxide 36 and 41 of a sacrifice layer is removed and a structure is formed, it is provided with sufficient corrosion resistance.

[0048]2) It is thought that the cause of the instability of electrical properties, such as a drift, is mainly the interface state density between the insulator layer 18 and the oxide film 19. Then, when the polysilicon film in which an interface state with the oxide film 19 is stable, and has tolerance strong against hydrofluoric acid instead of the insulator layer 18 was used, conventionally, in addition to the ordinary characteristic, the drift was almost lost and dispersion in threshold voltage was also able to be lessened.

[0049]In addition, if impurities, such as boron or Lynn, are introduced into the channel part of a polysilicon film, a threshold can be stabilized small.

[0050]2) Two of the followings are mainly one of causes of adhesion.

** The suction force between molecules (or atom) committed when the vibration gate 16 and the substrate 11 contact.

** Static electricity with which the insulator 19 is tinged by pouring an electric charge into the insulator 19 by causes, such as friction.

[0051]The following measures were performed as a method of solving these. ** If attached, the relation of the surface roughness of an attachment phenomenon and the substrate 11 was investigated, and when surface roughness was large, it solved using the ability of adhesion not to get up easily.

[0052]** If attached, it is the semi insulating polysilicon film to which at least one place was connected in the substrate 11 or the vibration gate 16, and solved by covering the surface of the substrate 11.

[0053]Gate dielectric film is protected, and the purpose of this invention can prevent a drift, and is to provide the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method.

[0054]

[Means for Solving the Problem]In an oscillating-type transducer which measures distortion added to both ends of this vibration gate when this invention measured resonance frequency of a vibration gate where (1) both ends were fixed to a substrate, in order to attain this purpose, A substrate of a semiconductor which has the 1st conduction type type, a drain which is formed in the surface of this substrate and has the 2nd conduction type type with said reverse conduction type type, and a channel inserted with sauce, This gate oxide [which was formed on the surface of said substrate], and gate oxide top A wrap polysilicon protective film, Are fixed to said substrate, and both ends cover, are arranged [hold a gap from the surface of this polysilicon protective film and], and said drain, sauce, and a channel so that it may consist of polysilicon and can be displaced by self-oscillation. An oscillating-type transducer possessing a tabular conductive vibration gate displaced according to electrostatic force produced between these drains.

(2) The oscillating-type transducer according to claim 1, wherein at least one place possesses a polysilicon protective film electrically connected to said semiconductor

substrate or said vibration gate.

(3) The oscillating-type transducer possessing a conduction part formed in a portion of said polysilicon protective film which counters said channel by spreading an impurity according to claim 1 or 2.

(4) The oscillating-type transducer possessing SHIERU by which an inside of a cover was held in said vibration gate at a vacuum according to claim 1, 2, or 3.

(5) A manufacturing method of an oscillating-type transducer having the following processes in a manufacturing method of an oscillating-type transducer which measures distortion added to both ends of this vibration gate when both ends measured resonance frequency of a vibration gate fixed to a substrate.

(a) A gate oxide formation process which forms gate oxide on a substrate of a semiconductor which has the 1st conduction type type.

(b) An ion implantation process which carries out the ion implantation of the impurity used as the 2nd conduction type type to a predetermined region corresponding to sauce, a drain, or a lead part of a gate.

(c) A polysilicon protection film formation process which forms a polysilicon protective film on said gate oxide.

(d) The 1st sacrifice layer oxide film formation process which forms the 1st sacrifice layer oxide film on this polysilicon protective film.

(e) Form a polysilicon film on this 1st sacrifice layer oxide film. Then, an impurity which serves as the 2nd conduction type type for addition of conductivity is doped. A beam building process of etching this polysilicon film and forming a beam corresponding to a vibration gate.

(f) The 2nd sacrifice layer oxide film formation process which forms the 2nd sacrifice layer oxide film on said 1st sacrifice layer oxide film and said beam.

(g) A gap corresponding point formation process which etches said 1st and 2nd sacrifice layer oxide film, and forms a gap corresponding point.

(h) A film formation process corresponding to a gap which forms an oxide film corresponding to a gap as a sacrifice layer in the whole surface including a said polysilicon protective film and gap corresponding point top.

(i) Form a polysilicon film on an oxide film corresponding to this gap. A shell corresponding point formation process which etches this polysilicon film and forms a shell corresponding point.

(j) An etching gap formation process of etching an oxide film corresponding to said gap, forming an introducing hole, and also removing said gap corresponding point via this introducing hole.

(k) A vacuum lock process of forming said said shell corresponding point, said introducing hole, and polysilicon protective film top with a polysilicon film, and holding an inside of shell to a vacuum in a vacuum.

(l) Carry out etching removal of some of said gate oxides in the upper part of said source part and said drain part, said polysilicon protective films, and said polysilicon films, carry out an opening, and form a contact hole. Then, an electrode formation process which forms a pad portion in this contact hole part, and wires by carrying out bonding by a gold streak.

(m) A diaphragm formation process which etches a pars basilaris ossis occipitalis of a substrate of a semiconductor which has said 1st conduction type type, and forms a diaphragm.

[0055]

[Embodiment of the Invention]Drawing 1 is an important section composition explanatory view of one example of this invention. In a figure, the composition of the same sign as drawing 20 expresses the same function. Hereafter, only drawing 20 and a different part are explained. 61 is a wrap polysilicon protective film about the gate oxide 19 top.

[0056]In the above composition, since electronegative potential is impressed to the vibration gate 16 which functions as a gate from DC power supply E2, it is pushed aside by the electron inside the silicon substrate 11 from the surface under the vibration gate 16, and an electron hole can be conversely drawn near to the surface.

[0057]Channel CNN2 which is a conduction layer of thin P type will be formed in the surface of the electron hole (P type) which was able to be drawn near, between the drains D (P type) will be connected with P type to the sauce S (P type), and, for this reason, current i_{d2} flows between the sauce S and the drain D.

[0058]The voltage of the drain D generated by this current i_{d2}, The electrostatic suction force between the vibration gate 16 and the drain D is changed by the electrical change which received the phase shift and received this phase shift by drain resistance R_D and electric capacity C_D formed between a drain and the silicon substrate 11, and interval x_2 is changed.

[0059]The thickness of channel CNN2 is changed by change of this interval x_2, current i_{d2} is changed by this, and this causes the electrical change of a drain. Although this is repeated and it oscillates, this oscillation is continued by selecting so that the product (omegaR_DC_D) of drain resistance R_D, the drain D and electric capacity C_D between the silicon substrates 11, and oscillation angular velocity omega of an oscillation may become very large compared with 1.

[0060]In the state where self-oscillation is maintained as mentioned above, if pressure P_M is impressed to the silicon substrate 11, distortion by this pressure P_M will be added to the vibration gate 16 via the fixed ends 14 and 15 which fix the vibration gate 16, and character frequency will change corresponding to this. Therefore, the value of pressure P_M is detectable by taking out change of this character frequency.

[0061]As a result, the polysilicon protective film 61 formed in the outermost surface of (1) board 11 structure, In [the corrosion resistance of hydrofluoric acid solution is enough, and] the manufacturing process of the vibration gate 16, at the time of sacrifice layer etching, the gate oxide 19 is exposed to hydrofluoric acid solution, and element structure is not destroyed.

[0062](2) Since the polysilicon protective film 61 can do an interface state with the gate oxide 19 good, dispersion in a threshold is pressed down and the oscillating-type transducer from which electric stability -- a drift hardly occurs -- is obtained is obtained.

[0063](3) If the polysilicon protective film 61 grows up thickness thickly, as for it, minute unevenness is made on the surface, and it can change surface roughness. The vibration gate 16 was able to make it hard to lower surface adhesion energy and to adhere by using the polysilicon protective film 61, as a result of investigating the relation between this surface roughness and adhesion by experiment.

[0064]At the process before separating the structure of the silicon of vibration gate 16 grade by sacrifice layer etching, since the polysilicon protective film 61 is formed, the vibration gate 16 can already be prevented from adhering to the silicon substrate 11 according to the sacrifice layer etching process of separation.

[0065]Since the sacrifice-layer-etching introducing hole 86 can be narrowed, in this structure at a vacuum lock process. The polysilicon 87 for a vacuum lock adheres to the peripheral face of the vibration gate 16, the remains tension distortion of the vibration gate 16 cannot be eased, or sectional shape cannot change thickly, and dispersion in the resonance frequency of the vibration gate 16 can be stopped small.

[0066]By next, the semi insulating polysilicon film protective film 61 electrically [at least one place] connected to the semiconductor substrate 11 or the vibration gate 16. By factors, such as static electricity, if the surface of the substrate 11 is covered, even if an electric charge is poured into the gate oxide 19, electrification of an electric charge can be suppressed and the oscillating-type transducer which can prevent adhesion on the substrate 11 of the vibration gate 16 and the wall surface of the shell 23 by static electricity can be obtained.

[0067]Next, if the conduction part by which the impurity was formed in the portion of the polysilicon protective film 61 which counters channel CNN2 by being spread is provided, the oscillating-type transducer which can stabilize a threshold small will be obtained.

[0068]The vibration gate 16 is covered, if SHIERU 23 by which the inside was held at the vacuum is formed, Q value of vibration of the vibration gate 16 can be made high, and a highly precise oscillating-type transducer can be obtained.

[0069]Next, the manufacturing method which manufactures the oscillating gauge 22 as a component of such an oscillating-type transducer is explained using the manufacturing process figure shown in drawing 15 from drawing 2.

[0070](1) Drawing 2 shows a gate oxide formation process. On the substrate 71 of the silicon single crystal of n form, the gate oxide 72 is formed at a thickness of about 500 A, for example.

[0071](2) Drawing 3 shows an ion implantation process. Here, as p type impurities, the ion implantation of the boron is carried out to the predetermined region corresponding to

the sauce 73, the drain 74, or the lead part of a gate, and it is made into it.

[0072](3) Drawing 4 is carrying out the ion implantation of the boron to the channel section 75 in the shallow depth if needed, and can control the resistance between the sauce 73-drains 74 again.

[0073](4) Drawing 5 shows a polysilicon protection film formation process. In this process, to the hydrofluoric acid (HF) used by a post process, it is strong, and the duty of the protective film of the gate oxide 72 is achieved, and tolerance forms the polysilicon protective film 76 which is a stable film on the gate oxide 72 by a thickness of about about 5000 A.

[0074](5) Drawing 6 shows the 1st sacrifice layer oxide film formation process. This process first, The 1st sacrifice layer oxide film 77 is formed on the polysilicon protective film 76 for example, by the CVD (Chemical Vapor Deposition) method at a thickness of about 5000 A as a sacrifice layer of the bottom for forming an opening in the circumference of a vibration gate eventually.

[0075](6) Drawing 7 shows a beam building process. This process is a previous process for forming the vibration gate 16 eventually. First, the polysilicon film 78 (not shown) is formed, for example by a thickness of about 1 micrometer on the 1st sacrifice layer oxide film 77. Then, boron is doped in order to give conductivity.

[0076]Next, after making a mask the portion corresponding to the vibration gate 16, with photolithographic technique by RIE (Reactive Ion Etching). The polysilicon 78 (not shown) is etched into predetermined shape, and the tabular beam 79 which serves as the vibration gate 16 eventually is formed.

[0077](7) Drawing 8 shows the 2nd sacrifice layer oxide film formation process. This process forms the 2nd sacrifice layer oxide film 81 on the 1st sacrifice layer oxide film 77 and the beam 79, for example with a CVD method at a thickness of about 5000 A as a sacrifice layer of the portion except the bottom for forming an opening in the circumference of the vibration gate 16 eventually first.

[0078](8) Drawing 9 shows a gap corresponding point formation process. First, with photolithography technique, in the center section of the vibration gate 16, after carrying out the mask of the neighborhood of the beam 79, the 1st sacrifice layer oxide film 77

and the 2nd sacrifice layer oxide film 81 of these circumferences are etched with hydrofluoric acid, and the gap corresponding point 82 is formed.

[0079](9) Drawing 10 shows the film formation process corresponding to a gap. This process is about about 500 A in thickness, and forms in the whole surface the oxide film 83 corresponding to the gap as a sacrifice layer for introducing an etching reagent used by a post process with a CVD method including the polysilicon protective film 76 and gap corresponding point 82 top.

[0080](10) Drawing 11 shows a shell corresponding point formation process. On the oxide film 83 corresponding to the gap formed by drawing 10, the polysilicon film 84 (not shown) is formed so that it may become a thickness of about 1 micrometer.

[0081]Then, a mask is carried out using photolithography technique, the polysilicon film 84 is etched by RIE, and the shell corresponding point 85 is formed in the range of a wrap size for the vibration gate 16.

[0082](11) Drawing 12 shows an etching gap formation process. Using hydrofluoric acid and etching the oxide film 83 corresponding to a gap, in order to form the vibration gate 16 and the shell corresponding point 85, this process removes this, forms the introducing hole 86 and, subsequently also removes the gap corresponding point 82 via this introducing hole 86. Thus, the vibration gate 16 and the shell corresponding point 85 are formed.

[0083](12) Drawing 13 shows a vacuum lock process. In a vacuum, this process forms the shell corresponding point 85, introducing hole 86, and polysilicon protective film 76 top by a thickness of about about 1 micrometer with the polysilicon film 87, and holds the inside of the shell 23 to a vacuum.

[0084](13) Drawing 14 shows the process of forming an electrode. The opening of some of gate oxides 72 in the upper part of the source part 73 and the drain part 74, polysilicon protective films 76, and polysilicon films 87 is carried out using photolithography technique and RIE, and the contact holes 88 and 89 are formed.

[0085]Then, aluminum is formed to the contact holes 88 and 89 by sputtering process, and the pad portions 91 and 92 are formed in them using photography art. It wires by carrying out bonding by a gold streak.

[0086](14) Drawing 15 shows a diaphragm formation process. The pars basilaris ossis occipitalis of the substrate 71 of a silicon single crystal is etched, and the diaphragm 24 is formed so that a center section may turn into a thin-walled part which becomes heavy-gage in the circumference with thin meat using potassium hydrate (KOH) liquid.

[0087]The above is a manufacturing method which covers the oscillating gauge 62 of an oscillating-type transducer by the shell 23, and forms the diaphragm 24.

[0088]According to the manufacturing method of above this inventions, gate dielectric film can be protected, a drift can be prevented and the manufacturing method of the oscillating-type transducer which can manufacture cheaply and certainly the oscillating-type transducer which can prevent adhesion of a vibration gate using the conventional semiconductor process can be obtained.

[0089]

[Effect of the Invention]As mentioned above, the polysilicon protective film which was formed in the outermost surface of (1) substrate structure according to the 1st claim of this invention as explained in detail with the example, In [the corrosion resistance of hydrofluoric acid solution is enough and] the manufacturing process of a vibration gate, at the time of sacrifice layer etching, gate oxide is exposed to hydrofluoric acid solution, and element structure is not destroyed.

[0090](2) Since the polysilicon protective film can do an interface state with gate oxide good, dispersion in a threshold is pressed down and the oscillating-type transducer from which electric stability -- a drift hardly occurs -- is obtained is obtained.

[0091](3) If a polysilicon protective film grows up thickness thickly, as for it, minute unevenness is made on the surface, and it can change surface roughness. As a result of investigating the relation between this surface roughness and adhesion by experiment, by using a polysilicon protective film, surface adhesion energy was able to be lowered and it was able to be made for a vibration gate not to adhere.

[0092]At the process before separating the structure of silicon, such as a vibration gate, by sacrifice layer etching, since the polysilicon protective film is formed, a vibration gate can already be prevented from adhering to a silicon substrate according to the sacrifice layer etching process of separation.

[0093]Since a sacrifice-layer-etching introducing hole can be narrowed, in this structure at a vacuum lock process. Polysilicon for a vacuum lock adheres to the peripheral face of a vibration gate, the remains tension distortion of a vibration gate cannot be eased, or sectional shape cannot change thickly, and dispersion in the resonance frequency of a vibration gate can be stopped small.

[0094]According to the 2nd claim of this invention, by factors, such as static electricity, even if an electric charge is poured into gate oxide, at least one place A semiconductor substrate, Or by the semi insulating polysilicon film protective film electrically connected to the vibration gate, electrification of an electric charge can be suppressed for the gate oxide surface by a wrap, and the oscillating-type transducer which can prevent adhesion in the substrate and shell wall side of a vibration gate by static electricity can be obtained.

[0095]Since the conduction part by which the impurity was formed in the portion of the polysilicon film which counters a channel by being spread was provided according to the 3rd claim of this invention, the oscillating-type transducer which can stabilize a threshold small is obtained.

[0096]Since SHIERU by which the inside of a cover was held in the vibration gate at the vacuum was provided according to the 4th claim of this invention, Q value of vibration of a vibration gate can be made high, and a highly precise oscillating-type transducer can be obtained.

[0097]According to the 5th claim of this invention, gate dielectric film can be protected, a drift can be prevented and the manufacturing method of the oscillating-type transducer which can manufacture cheaply and certainly the oscillating-type transducer which can prevent adhesion of a vibration gate using the conventional semiconductor process can be obtained.

[0098]Therefore, according to this invention, gate dielectric film can be protected, a drift can be prevented and the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method can be realized.

TECHNICAL FIELD

[Field of the Invention]Gate dielectric film is protected, and this invention can prevent a drift, and relates to the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method.

PRIOR ART

[Description of the Prior Art]Drawing 16 is a theoretic composition explanatory view of the conventional example currently generally used conventionally, is the example using the oscillating-type transducer as a pressure sensor, and is shown in JP,7-30128,A, for example.

[0003]As for the silicon substrate 1, for example, a conduction type type is formed in n form, the electrode 2 is fixed here, and the electrode 2 is connected to common potential point COM. The impurity of p form is spread on the upper surface of this silicon substrate 1, the sauce S is formed in it, and the electrode 3 for taking out the potential of the sauce S here is formed in it. Pressure P_M which should be measured is impressed to the undersurface of this silicon substrate 1.

[0004]Only the prescribed interval W is left to this sauce S, similarly the impurity of p form is spread on the upper surface of the silicon substrate 1, the drain D is formed, and the electrode 4 for taking out the potential of the drain D is formed here.

[0005]Only x_1 is left above the portion of the prescribed interval W of the silicon substrate 1, the heights 5 and 6 are formed in it, and the both ends of the vibration gate 7 (the numerals which G become expedient may be used) which functions as a tabular vibrator to which the impurity was spread and conductivity was given are being fixed to the heights 5 and 6, such as this.

[0006]That is, although only x_1 is left and arranged except for both ends and the vibration gate 7 and the silicon substrate 1 are not illustrated by the silicon substrate 1 corresponding to this vibration gate 7, channel CNN1 is formed between the drain D and

the sauce S.

[0007]Between the electrode 4 and common potential point COM, the resistance R1 and DC power supply E1 are connected in series, and the potential of the drain D is held to common potential point COM at negative potential. It is connected to the vibration gate 7 so that DC power supply E2 may become negative potential to common potential point COM.

[0008]Drawing 17 is an explanatory view explaining operation of drawing 16. It has composition including the section of the silicon substrate 1 seen from the longitudinal direction of the vibration gate 7. Since electronegative potential is impressed to the vibration gate 7 which functions as a gate from DC power supply E2, as shown in drawing 17, it is pushed aside by the electron inside the silicon substrate 1 (drawing 17 the lower one) from the surface under the vibrator 7, and an electron hole can be conversely drawn near to the surface.

[0009]Channel CNN1 which is a conduction layer of thin P type will be formed in the surface of the electron hole (P type) which was able to be drawn near, between the drains D (P type) will be connected with P type to the sauce S (P type), and, for this reason, current i_{d1} flows between the sauce S and the drain D.

[0010]The voltage of the drain D generated by this current i_{d1}, The electrostatic suction force between the vibration gate 7 and the drain D is changed by the electrical change which received the phase shift and received this phase shift by drain resistance R_D and electric capacity C_D formed between a drain and the silicon substrate 1, and interval x_1 is changed.

[0011]The thickness of channel CNN1 is changed by change of this interval x_1, current i_{d1} is changed by this, and this causes the electrical change of a drain. Although this is repeated and it oscillates, this oscillation is continued by selecting so that the product (omegaR_DC_D) of drain resistance R_D, the drain D and electric capacity C_D between the silicon substrates 1, and oscillation angular velocity omega of an oscillation may become very large compared with 1.

[0012]In the state where self-oscillation is maintained as mentioned above, if pressure P_M is impressed to the silicon substrate 1 like a graphic display, distortion by this

pressure P_M will be added to the vibration gate 7 via the heights 5 and 6 which fix the vibration gate 7, and character frequency will change corresponding to this. Therefore, the value of pressure P_M is detectable by taking out change of this character frequency.

[0013]The perspective view and drawing 19 which drawing 18 shows the composition of the concrete example of drawing 16 are a sectional view near [the] the center section. However, the vibration gate is omitted about wrap shell portions and a diaphragm portion. Drawing 20 is a whole sectional side elevation in the center portion of a vibration gate.

[0014]In drawing 18, drawing 19, and drawing 20, the silicon substrate 11, For example, a conduction type type is formed in n form, the impurity of p form is spread on the upper surface of this silicon substrate 11, the sauce S is formed in it, and the electrode 12 made from aluminum for taking out the potential of the sauce S is formed here via wiring section W_S shown by a dotted line. Although not illustrated in the undersurface of this silicon substrate 11, pressure P_M which a diaphragm is formed in recessed shape and should measure here is impressed.

[0015]Only a prescribed interval is left to this sauce S, similarly the impurity of p form is spread on the upper surface of the silicon substrate 11, the drain D is formed, and the electrode 13 made from aluminum for taking out the potential of the drain D is formed here via wiring section W_D shown by a dotted line.

[0016]Only gap x_2 is left above the silicon substrate 11, the fixed ends 14 and 15 are formed in it, and the both ends of the tabular vibration gate 16 of the polysilicon in which the impurity was spread and conductivity was given are being fixed to the fixed ends 14 and 15, such as this, by one. The length of the beam of the vibration gate 16 is L. And this vibration gate 16 is connected via wiring part W_G shown by the electrode 17 and dotted line made from aluminum.

[0017]That is, except for both ends, the vibration gate 16 and the silicon substrate 11 leave only gap x_2, and are arranged, and channel CNN2 is formed between the drain D of the silicon substrate 11 and the sauce S corresponding to this vibration gate 16.

[0018]These drain [that were formed in the upper surface of the silicon substrate 11] D, and channel CNN2, and the corrosion-resistant high protective film [as opposed to hydrofluoric acid (HF) in the sauce S top] 18, for example, $S_{i3}N_4$, The two-layer structure

film 21 which consists of $S_iC_xN_y$, S_iC, AL_2O_3, etc. and the oxide film 19 is formed. The protective film 18 is the same insulator as the oxide film 19.

[0019]And between this two-layer structure film 21 and vibration gate 16, the gap is provided so that the vibration gate 16 can vibrate up and down considering the fixed ends 14 and 15 as a paragraph. Thus, the oscillating gauge 22 is constituted. 23 is SHIERU and 24 is a diaphragm.

[0020]The point which combines an oscillating gauge and an electronic circuit as shown in drawing 18, and constitutes an oscillating-type transducer from old explanation was explained. Next, the manufacturing method which manufactures the oscillating gauge 22 as a component of such an oscillating-type transducer is explained using the manufacturing process figure shown in drawing 21 and drawing 22.

[0021]Although the manufacturing process shown in drawing 22 continues succeeding the manufacturing process shown in drawing 21, it is divided into two on [of explanation] expedient. In the composition shown in drawing 18, since the section structures produced in process of a manufacturing process in the portion of the vibration gate 16 and the portion of the fixed ends 14 and 15 which fix this at both ends differ, although it is the same process, it separates into right and left and these are illustrated according to each.

[0022]In the section structure of the center section of the vibration gate 16, the right-hand side figure of the chart on the left is the section structure of the portion of the fixed end 14. Since the portion of the fixed end 15 is the same structure as the portion of the fixed end 14, it is omitted.

[0023]Step 1 shows a gate oxide formation process. The gate oxide 31 is formed on the substrate 30 of the silicon single crystal of n form at a thickness of about 500 A, for example. In this process, the section structure in the center section and fixed end part of a vibration gate is formed identically. Then, it shifts to Step 2. Henceforth, each step is gone on according to a step number.

[0024]Step 2 shows an ion implantation process. Here, the ion implantation of the boron is carried out to a predetermined region as p type impurities. This sets prescribed interval W_N which is due to form channel CCN in the center section of the vibration gate,

and the source part 32 (it corresponds to W_S of drawing 18) and the drain part 33 (it corresponds to W_D of drawing 18) of p form are formed, In a fixed end part, the gate lead part 34 (it corresponds to W_G of drawing 18) of p form is formed.

[0025]Step 3 shows a channel formation process. Here, the ion implantation of the boron is carried out to the channel section 34 (CCN2) of prescribed interval W_N which is due to form channel CCN in the center section of the vibration gate in the shallow depth. Resistance between source drains is controllable by this to a predetermined value. In this case, it is changeless in a fixed end part.

[0026]Step 4 shows a nitride formation process. In this process, for the protection of the gate oxide 31 to the hydrofluoric acid (HF) used by a post process, As the strong insulator layer 35, tolerance forms an $S_iC_xN_y$ film on the gate oxide 31 by a thickness of about about 1000 A to hydrofluoric acid, for example.

[0027]Step 5 shows the 1st sacrifice layer oxide film formation process. This process forms the oxide film 36 on the insulator layer 35 by the CVD (Chemical Vapour Deposition) method at a thickness of about 5000 A as a sacrifice layer of the bottom for forming an opening in the circumference of the vibration gate 16 eventually first.

[0028]Next, to a fixed end part, the portions of the gate oxide 31 of the portion of the schedule in which the fixed end 14 is formed by photolithographic technique, the insulator layer 35, and the oxide film 36 are used as the opening 37, and an opening is carried out.

[0029]Step 6 shows polysilicon stage film formation. This process is a previous process for forming the vibration gate 16 and the fixed end 14 eventually. First, the polysilicon 38 is formed by a thickness of about 1 micrometer on the oxide film 36 and the opening 37. Then, boron is doped in order to give conductivity.

[0030]Next, after making a mask the portion corresponding to the vibration gate 16, and the portion corresponding to the opening 37 with photolithographic technique, The support 40 of a Y-globe type is formed in the tabular beam 39 which etches the polysilicon 38 into predetermined shape by RIE (Reactive Ion Etching), and serves as a vibration gate eventually, and the opening 37.

[0031]Step 7 shows the 2nd sacrifice layer oxide film formation process. This process

forms the oxide film 41 on the oxide film 36, the beam 39, and the support 40 with a CVD method at a thickness of about 5000 A as a sacrifice layer of the portion except the bottom for forming an opening in the circumference of the vibration gate 16 eventually.

[0032]Step 8 shows an oxide film etching process. First, after carrying out the mask of the portion remove the neighborhood of the beam 39 in the center section of the vibration gate, and excluding Y character center section 42 of the support 40 near the support 40 in a fixed end part with photolithographic technique, the oxide films 36 and 41 of these circumferences are etched with hydrofluoric acid, and the gap corresponding points 43 and 44 are formed.

[0033]Step 9 shows the stage film formation corresponding to a gap. This process forms in the whole surface the oxide film 45 as a sacrifice layer for introducing the etching reagent used by a post process with a CVD method including the insulator layer 35 and gap corresponding point 43 and 44 top by a thickness of about about 500 A. Then, the oxide film 45 on Y character center section 42 is etched and removed using photolithographic technique.

[0034]Step 10 shows a SHIERU corresponding point formation process. The polysilicon 46 is formed so that it may become a thickness of about 1 micrometer on the oxide film 45 etc. which were formed at Step 9. Then, short time heat treatment of the stress which remains in polysilicon of SHIERU and a vibration gate by RTA (Rapid Thermal Aneal) is carried out, it is removed, and these are prevented from changing.

[0035]Then, a mask is carried out using photolithographic technique, the polysilicon 46 is etched by RIE, and the SHIERU corresponding point 47 is formed in the range of a wrap size for a vibration gate.

[0036]Step 11 shows an etching gap formation process. In order to form a vibration gate and SHIERU, using hydrofluoric acid and etching the oxide film 45, this process removes this, forms the introducing hole 48 and, subsequently also removes the gap corresponding points 43 and 44 via this introducing hole 48. Thus, the vibration gate 16, the fixed end 14, and SHIERU 49 are formed.

[0037]Step 12 shows a vacuum lock process. This process forms the SHIERU 49, introducing hole 48, and insulator layer 35 top by a thickness of about about 5000 A with

the polysilicon 50 in a vacuum, and holds the inside of SHIERU 49 to a vacuum.

[0038]Step 13 shows a contact hole formation process. The opening of some of gate oxides 31 in the upper part of the source part 32 and the drain part 33, insulator layers 35, and polysilicon 50 is carried out using photolithographic technique and RIE, and the contact holes 51 and 52 are formed. Similarly, the contact hole 54 can be formed also in a gate section.

[0039]Step 14 shows a diaphragm formation process. The pars basilaris ossis occipitalis of the substrate 30 of a silicon single crystal is etched, and the diaphragm 53 is formed so that a center section may turn into a thin-walled part which becomes heavy-gage in the circumference with thin meat using potassium hydrate (KOH) liquid.

[0040]Step 15 shows a bonding process. The electrodes 13 and 12 made from aluminum are formed in the contact holes 51 and 52. The above is a manufacturing method which covers the oscillating gauge of an oscillating-type transducer by shell, and forms a diaphragm.

EFFECT OF THE INVENTION

[Effect of the Invention]As mentioned above, the polysilicon protective film which was formed in the outermost surface of (1) substrate structure according to the 1st claim of this invention as explained in detail with the example, In [the corrosion resistance of hydrofluoric acid solution is enough and] the manufacturing process of a vibration gate, at the time of sacrifice layer etching, gate oxide is exposed to hydrofluoric acid solution, and element structure is not destroyed.

[0090](2) Since the polysilicon protective film can do an interface state with gate oxide good, dispersion in a threshold is pressed down and the oscillating-type transducer from which electric stability -- a drift hardly occurs -- is obtained is obtained.

[0091](3) If a polysilicon protective film grows up thickness thickly, as for it, minute unevenness is made on the surface, and it can change surface roughness. As a result of investigating the relation between this surface roughness and adhesion by experiment,

by using a polysilicon protective film, surface adhesion energy was able to be lowered and it was able to be made for a vibration gate not to adhere.

[0092]At the process before separating the structure of silicon, such as a vibration gate, by sacrifice layer etching, since the polysilicon protective film is formed, a vibration gate can already be prevented from adhering to a silicon substrate according to the sacrifice layer etching process of separation.

[0093]Since a sacrifice-layer-etching introducing hole can be narrowed, in this structure at a vacuum lock process. Polysilicon for a vacuum lock adheres to the peripheral face of a vibration gate, the remains tension distortion of a vibration gate cannot be eased, or sectional shape cannot change thickly, and dispersion in the resonance frequency of a vibration gate can be stopped small.

[0094]According to the 2nd claim of this invention, by factors, such as static electricity, even if an electric charge is poured into gate oxide, at least one place A semiconductor substrate, Or by the semi insulating polysilicon film protective film electrically connected to the vibration gate, electrification of an electric charge can be suppressed for the gate oxide surface by a wrap, and the oscillating-type transducer which can prevent adhesion in the substrate and shell wall side of a vibration gate by static electricity can be obtained.

[0095]Since the conduction part by which the impurity was formed in the portion of the polysilicon film which counters a channel by being spread was provided according to the 3rd claim of this invention, the oscillating-type transducer which can stabilize a threshold small is obtained.

[0096]Since SHIERU by which the inside of a cover was held in the vibration gate at the vacuum was provided according to the 4th claim of this invention, Q value of vibration of a vibration gate can be made high, and a highly precise oscillating-type transducer can be obtained.

[0097]According to the 5th claim of this invention, gate dielectric film can be protected, a drift can be prevented and the manufacturing method of the oscillating-type transducer which can manufacture cheaply and certainly the oscillating-type transducer which can prevent adhesion of a vibration gate using the conventional semiconductor

process can be obtained.

[0098]Therefore, according to this invention, gate dielectric film can be protected, a drift can be prevented and the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method can be realized.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, there are the following problems in such a structural form transducer formed on the semiconductor substrate using ultra-fine processing technology (micromachining).

[0042]1) In order to use the silicon oxide 36 and 41 for a sacrifice layer at the process of producing structures, such as the vibration gate 16, it is necessary to etch with hydrofluoric acid at the process of removing this for a long time. Although it is necessary to protect the film which I do not want to provide in the silicon substrate 11 side and to etch the gate oxide 19 required as an insulator layer etc. at this time by the gate oxide 19 and the high protective film 18 of hydrofluoric acid-proof nature of the same silicon nitride film 18 grade that is an insulating material, Sufficient corrosion resistance was not acquired.

[0043]2) Furthermore, if the gate oxide 19 is protected by the high protective film of hydrofluoric acid-proof nature, such as a silicon nitrogen-ized film, since level is made to an interface with the gate oxide 19, by the film of silicon nitride film 18 grade, The absolute value of the threshold voltage of the portion equivalent to FET becomes large, and and ********** and variation become large. Since the level of this interface is unstable, it causes degradation of electrical properties, such as a drift.

[0044]In this structure, since the electrode section equivalent to the gate of the usual MOSFET is not in contact with an insulator layer, a result which an electric potential gradient occurs, and the potential near the sauce falls horizontally in an insulator layer, therefore pushes up threshold voltage has been brought.

[0045]For this reason, when the operating point was fixed, the size of drain current had

a problem out of which dispersion comes or which a drift produces.

3) There is a problem that the vibration gate 16 will adhere to the silicon substrate 11, working [in a manufacturing process or after completion], and rigid small beam structure was seldom able to be produced.

[0046]However, if it is going to acquire a big frequency change rate when it is going to produce the oscillating-type sensor of the high sensitivity which has beam structure, Although thickness must be made [length / of a beam] thin, since such a beam had small rigidity and it adhered to a silicon substrate easily for a long time, it was difficult to produce a high sensitivity oscillating-type sensor.

[0047]The following solutions were adopted to the above problems.

1) The corrosion resistance of a polysilicon film over hydrofluoric acid solution is strong enough as compared with silicon nitride film 18 grade, and although the silicon oxide 36 and 41 of a sacrifice layer is removed and a structure is formed, it is provided with sufficient corrosion resistance.

[0048]2) It is thought that the cause of the instability of electrical properties, such as a drift, is mainly the interface state density between the insulator layer 18 and the oxide film 19. Then, when the polysilicon film in which an interface state with the oxide film 19 is stable, and has tolerance strong against hydrofluoric acid instead of the insulator layer 18 was used, conventionally, in addition to the ordinary characteristic, the drift was almost lost and dispersion in threshold voltage was also able to be lessened.

[0049]In addition, if impurities, such as boron or Lynn, are introduced into the channel part of a polysilicon film, a threshold can be stabilized small.

[0050]2) Two of the followings are mainly one of causes of adhesion.

** The suction force between molecules (or atom) committed when the vibration gate 16 and the substrate 11 contact.

** Static electricity with which the insulator 19 is tinged by pouring an electric charge into the insulator 19 by causes, such as friction.

[0051]The following measures were performed as a method of solving these. ** If attached, the relation of the surface roughness of an attachment phenomenon and the substrate 11 was investigated, and when surface roughness was large, it solved using the

ability of adhesion not to get up easily.

[0052]** If attached, it is the semi insulating polysilicon film to which at least one place was connected in the substrate 11 or the vibration gate 16, and solved by covering the surface of the substrate 11.

[0053]Gate dielectric film is protected, and the purpose of this invention can prevent a drift, and is to provide the oscillating-type transducer which can prevent adhesion of a vibration gate, and its manufacturing method.

MEANS

[Means for Solving the Problem]In an oscillating-type transducer which measures distortion added to both ends of this vibration gate when this invention measured resonance frequency of a vibration gate where (1) both ends were fixed to a substrate, in order to attain this purpose, A substrate of a semiconductor which has the 1st conduction type type, a drain which is formed in the surface of this substrate and has the 2nd conduction type type with said reverse conduction type type, and a channel inserted with sauce, This gate oxide [which was formed on the surface of said substrate], and gate oxide top A wrap polysilicon protective film, Are fixed to said substrate, and both ends cover, are arranged [hold a gap from the surface of this polysilicon protective film and], and said drain, sauce, and a channel so that it may consist of polysilicon and can be displaced by self-oscillation. An oscillating-type transducer possessing a tabular conductive vibration gate displaced according to electrostatic force produced between these drains.

(2) The oscillating-type transducer according to claim 1, wherein at least one place possesses a polysilicon protective film electrically connected to said semiconductor substrate or said vibration gate.

(3) The oscillating-type transducer possessing a conduction part formed in a portion of said polysilicon protective film which counters said channel by spreading an impurity according to claim 1 or 2.

(4) The oscillating-type transducer possessing SHIERU by which an inside of a cover was held in said vibration gate at a vacuum according to claim 1, 2, or 3.

(5) A manufacturing method of an oscillating-type transducer having the following processes in a manufacturing method of an oscillating-type transducer which measures distortion added to both ends of this vibration gate when both ends measured resonance frequency of a vibration gate fixed to a substrate.

(a) A gate oxide formation process which forms gate oxide on a substrate of a semiconductor which has the 1st conduction type type.

(b) An ion implantation process which carries out the ion implantation of the impurity used as the 2nd conduction type type to a predetermined region corresponding to sauce, a drain, or a lead part of a gate.

(c) A polysilicon protection film formation process which forms a polysilicon protective film on said gate oxide.

(d) The 1st sacrifice layer oxide film formation process which forms the 1st sacrifice layer oxide film on this polysilicon protective film.

(e) Form a polysilicon film on this 1st sacrifice layer oxide film. Then, an impurity which serves as the 2nd conduction type type for addition of conductivity is doped. A beam building process of etching this polysilicon film and forming a beam corresponding to a vibration gate.

(f) The 2nd sacrifice layer oxide film formation process which forms the 2nd sacrifice layer oxide film on said 1st sacrifice layer oxide film and said beam.

(g) A gap corresponding point formation process which etches said 1st and 2nd sacrifice layer oxide film, and forms a gap corresponding point.

(h) A film formation process corresponding to a gap which forms an oxide film corresponding to a gap as a sacrifice layer in the whole surface including a said polysilicon protective film and gap corresponding point top.

(i) Form a polysilicon film on an oxide film corresponding to this gap. A shell corresponding point formation process which etches this polysilicon film and forms a shell corresponding point.

(j) An etching gap formation process of etching an oxide film corresponding to said gap,

forming an introducing hole, and also removing said gap corresponding point via this introducing hole.

(k) A vacuum lock process of forming said said shell corresponding point, said introducing hole, and polysilicon protective film top with a polysilicon film, and holding an inside of shell to a vacuum in a vacuum.

(l) Carry out etching removal of some of said gate oxides in the upper part of said source part and said drain part, said polysilicon protective films, and said polysilicon films, carry out an opening, and form a contact hole. Then, an electrode formation process which forms a pad portion in this contact hole part, and wires by carrying out bonding by a gold streak.

(m) A diaphragm formation process which etches a pars basilaris ossis occipitalis of a substrate of a semiconductor which has said 1st conduction type type, and forms a diaphragm.

[0055]

[Embodiment of the Invention]Drawing 1 is an important section composition explanatory view of one example of this invention. In a figure, the composition of the same sign as drawing 20 expresses the same function. Hereafter, only drawing 20 and a different part are explained. 61 is a wrap polysilicon protective film about the gate oxide 19 top.

[0056]In the above composition, since electronegative potential is impressed to the vibration gate 16 which functions as a gate from DC power supply E2, it is pushed aside by the electron inside the silicon substrate 11 from the surface under the vibration gate 16, and an electron hole can be conversely drawn near to the surface.

[0057]Channel CNN2 which is a conduction layer of thin P type will be formed in the surface of the electron hole (P type) which was able to be drawn near, between the drains D (P type) will be connected with P type to the sauce S (P type), and, for this reason, current i_{d2} flows between the sauce S and the drain D.

[0058]The voltage of the drain D generated by this current i_{d2}, The electrostatic suction force between the vibration gate 16 and the drain D is changed by the electrical change which received the phase shift and received this phase shift by drain resistance R_D and electric capacity C_D formed between a drain and the silicon substrate 11, and interval x_2

is changed.

[0059]The thickness of channel CNN2 is changed by change of this interval x_2, current i_{d2} is changed by this, and this causes the electrical change of a drain. Although this is repeated and it oscillates, this oscillation is continued by selecting so that the product (omega$R_D C_D$) of drain resistance R_D, the drain D and electric capacity C_D between the silicon substrates 11, and oscillation angular velocity omega of an oscillation may become very large compared with 1.

[0060]In the state where self-oscillation is maintained as mentioned above, if pressure P_M is impressed to the silicon substrate 11, distortion by this pressure P_M will be added to the vibration gate 16 via the fixed ends 14 and 15 which fix the vibration gate 16, and character frequency will change corresponding to this. Therefore, the value of pressure P_M is detectable by taking out change of this character frequency.

[0061]As a result, the polysilicon protective film 61 formed in the outermost surface of (1) board 11 structure, In [the corrosion resistance of hydrofluoric acid solution is enough, and] the manufacturing process of the vibration gate 16, at the time of sacrifice layer etching, the gate oxide 19 is exposed to hydrofluoric acid solution, and element structure is not destroyed.

[0062](2) Since the polysilicon protective film 61 can do an interface state with the gate oxide 19 good, dispersion in a threshold is pressed down and the oscillating-type transducer from which electric stability -- a drift hardly occurs -- is obtained is obtained.

[0063](3) If the polysilicon protective film 61 grows up thickness thickly, as for it, minute unevenness is made on the surface, and it can change surface roughness. The vibration gate 16 was able to make it hard to lower surface adhesion energy and to adhere by using the polysilicon protective film 61, as a result of investigating the relation between this surface roughness and adhesion by experiment.

[0064]At the process before separating the structure of the silicon of vibration gate 16 grade by sacrifice layer etching, since the polysilicon protective film 61 is formed, the vibration gate 16 can already be prevented from adhering to the silicon substrate 11 according to the sacrifice layer etching process of separation.

[0065]Since the sacrifice-layer-etching introducing hole 86 can be narrowed, in this structure at a vacuum lock process. The polysilicon 87 for a vacuum lock adheres to the peripheral face of the vibration gate 16, the remains tension distortion of the vibration gate 16 cannot be eased, or sectional shape cannot change thickly, and dispersion in the resonance frequency of the vibration gate 16 can be stopped small.

[0066]By next, the semi insulating polysilicon film protective film 61 electrically [at least one place] connected to the semiconductor substrate 11 or the vibration gate 16. By factors, such as static electricity, if the surface of the substrate 11 is covered, even if an electric charge is poured into the gate oxide 19, electrification of an electric charge can be suppressed and the oscillating-type transducer which can prevent adhesion on the substrate 11 of the vibration gate 16 and the wall surface of the shell 23 by static electricity can be obtained.

[0067]Next, if the conduction part by which the impurity was formed in the portion of the polysilicon protective film 61 which counters channel CNN2 by being spread is provided, the oscillating-type transducer which can stabilize a threshold small will be obtained.

[0068]The vibration gate 16 is covered, if SHIERU 23 by which the inside was held at the vacuum is formed, Q value of vibration of the vibration gate 16 can be made high, and a highly precise oscillating-type transducer can be obtained.

[0069]Next, the manufacturing method which manufactures the oscillating gauge 22 as a component of such an oscillating-type transducer is explained using the manufacturing process figure shown in drawing 15 from drawing 2.

[0070](1) Drawing 2 shows a gate oxide formation process. On the substrate 71 of the silicon single crystal of n form, the gate oxide 72 is formed at a thickness of about 500 A, for example.

[0071](2) Drawing 3 shows an ion implantation process. Here, as p type impurities, the ion implantation of the boron is carried out to the predetermined region corresponding to the sauce 73, the drain 74, or the lead part of a gate, and it is made into it.

[0072](3) Drawing 4 is carrying out the ion implantation of the boron to the channel section 75 in the shallow depth if needed, and can control the resistance between the sauce 73-drains 74 again.

[0073](4) Drawing 5 shows a polysilicon protection film formation process. In this process, to the hydrofluoric acid (HF) used by a post process, it is strong, and the duty of the protective film of the gate oxide 72 is achieved, and tolerance forms the polysilicon protective film 76 which is a stable film on the gate oxide 72 by a thickness of about about 5000 A.

[0074](5) Drawing 6 shows the 1st sacrifice layer oxide film formation process. This process first, The 1st sacrifice layer oxide film 77 is formed on the polysilicon protective film 76 for example, by the CVD (Chemical Vapor Deposition) method at a thickness of about 5000 A as a sacrifice layer of the bottom for forming an opening in the circumference of a vibration gate eventually.

[0075](6) Drawing 7 shows a beam building process. This process is a previous process for forming the vibration gate 16 eventually. First, the polysilicon film 78 (not shown) is formed, for example by a thickness of about 1 micrometer on the 1st sacrifice layer oxide film 77. Then, boron is doped in order to give conductivity.

[0076]Next, after making a mask the portion corresponding to the vibration gate 16, with photolithographic technique by RIE (Reactive Ion Etching). The polysilicon 78 (not shown) is etched into predetermined shape, and the tabular beam 79 which serves as the vibration gate 16 eventually is formed.

[0077](7) Drawing 8 shows the 2nd sacrifice layer oxide film formation process. This process forms the 2nd sacrifice layer oxide film 81 on the 1st sacrifice layer oxide film 77 and the beam 79, for example with a CVD method at a thickness of about 5000 A as a sacrifice layer of the portion except the bottom for forming an opening in the circumference of the vibration gate 16 eventually first.

[0078](8) Drawing 9 shows a gap corresponding point formation process. First, with photolithography technique, in the center section of the vibration gate 16, after carrying out the mask of the neighborhood of the beam 79, the 1st sacrifice layer oxide film 77 and the 2nd sacrifice layer oxide film 81 of these circumferences are etched with hydrofluoric acid, and the gap corresponding point 82 is formed.

[0079](9) Drawing 10 shows the film formation process corresponding to a gap. This process is about about 500 A in thickness, and forms in the whole surface the oxide film

83 corresponding to the gap as a sacrifice layer for introducing an etching reagent used by a post process with a CVD method including the polysilicon protective film 76 and gap corresponding point 82 top.

[0080](10) Drawing 11 shows a shell corresponding point formation process. On the oxide film 83 corresponding to the gap formed by drawing 10, the polysilicon film 84 (not shown) is formed so that it may become a thickness of about 1 micrometer.

[0081]Then, a mask is carried out using photolithography technique, the polysilicon film 84 is etched by RIE, and the shell corresponding point 85 is formed in the range of a wrap size for the vibration gate 16.

[0082](11) Drawing 12 shows an etching gap formation process. Using hydrofluoric acid and etching the oxide film 83 corresponding to a gap, in order to form the vibration gate 16 and the shell corresponding point 85, this process removes this, forms the introducing hole 86 and, subsequently also removes the gap corresponding point 82 via this introducing hole 86. Thus, the vibration gate 16 and the shell corresponding point 85 are formed.

[0083](12) Drawing 13 shows a vacuum lock process. In a vacuum, this process forms the shell corresponding point 85, introducing hole 86, and polysilicon protective film 76 top by a thickness of about about 1 micrometer with the polysilicon film 87, and holds the inside of the shell 23 to a vacuum.

[0084](13) Drawing 14 shows the process of forming an electrode. The opening of some of gate oxides 72 in the upper part of the source part 73 and the drain part 74, polysilicon protective films 76, and polysilicon films 87 is carried out using photolithography technique and RIE, and the contact holes 88 and 89 are formed.

[0085]Then, aluminum is formed to the contact holes 88 and 89 by sputtering process, and the pad portions 91 and 92 are formed in them using photography art. It wires by carrying out bonding by a gold streak.

[0086](14) Drawing 15 shows a diaphragm formation process. The pars basilaris ossis occipitalis of the substrate 71 of a silicon single crystal is etched, and the diaphragm 24 is formed so that a center section may turn into a thin-walled part which becomes heavy-gage in the circumference with thin meat using potassium hydrate (KOH) liquid.

[0087]The above is a manufacturing method which covers the oscillating gauge 62 of an oscillating-type transducer by the shell 23, and forms the diaphragm 24.

[0088]According to the manufacturing method of above this inventions, gate dielectric film can be protected, a drift can be prevented and the manufacturing method of the oscillating-type transducer which can manufacture cheaply and certainly the oscillating-type transducer which can prevent adhesion of a vibration gate using the conventional semiconductor process can be obtained.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is an important section composition explanatory view of one example of this invention.

[Drawing 2]It is a gate oxide formation process explanatory view of drawing 1.

[Drawing 3]It is an ion implantation process explanatory view of drawing 1.

[Drawing 4]It is an ion implantation process explanatory view of drawing 1.

[Drawing 5]It is a polysilicon protection film formation process explanatory view of drawing 1.

[Drawing 6]It is the 1st sacrifice layer oxide film formation process explanatory view of drawing 1.

[Drawing 7]It is a beam building routing description figure of drawing 1.

[Drawing 8]It is the 2nd sacrifice layer oxide film formation process explanatory view of drawing 1.

[Drawing 9]It is a gap corresponding point formation process explanatory view of drawing 1.

[Drawing 10]It is a film formation routing description figure corresponding to the gap of drawing 1.

[Drawing 11]It is a shell corresponding point formation process explanatory view of drawing 1.

[Drawing 12]It is an etching gap formation routing description figure of drawing 1.

[Drawing 13]It is a vacuum lock routing description figure of drawing 1.

[Drawing 14]It is an electrode formation process explanatory view of drawing 1.

[Drawing 15]It is a diaphragm formation process explanatory view of drawing 1.

[Drawing 16]It is a theoretic composition explanatory view of the conventional example currently generally used conventionally.

[Drawing 17]It is an explanatory view of drawing 16 of operation.

[Drawing 18]It is a perspective view showing the composition of the concrete example of drawing 16.

[Drawing 19]It is a sectional view near the center section of drawing 18.

[Drawing 20]It is a whole sectional side elevation in the center portion of the vibration gate 16 of drawing 18.

[Drawing 21]It is a manufacturing process explanatory view of drawing 18.

[Drawing 22]It is a manufacturing process explanatory view of drawing 18.

[Description of Notations]

11 Silicon substrate

12 Electrode

13 Electrode

14 Fixed end

15 Fixed end

16 Vibration gate

17 Electrode

19 Gate oxide

21 Two-layer structure film

22 Oscillating gauge

23 Shell

24 Diaphragm

61 Polysilicon protective film

71 Silicon substrate

72 Gate oxide

73 Sauce

74 Drain

75 Channel section

76 Polysilicon protective film

77 The 1st sacrifice layer oxide film

78 Polysilicon

79 Beam

81 The 2nd sacrifice layer oxide film

82 Gap corresponding point

83 The oxide film corresponding to a gap

84 Polysilicon film

85 Shell corresponding point

86 Introducing hole

87 Polysilicon film

88 Contact hole

89 Contact hole

91 Pad portion

92 Pad portion

S Sauce

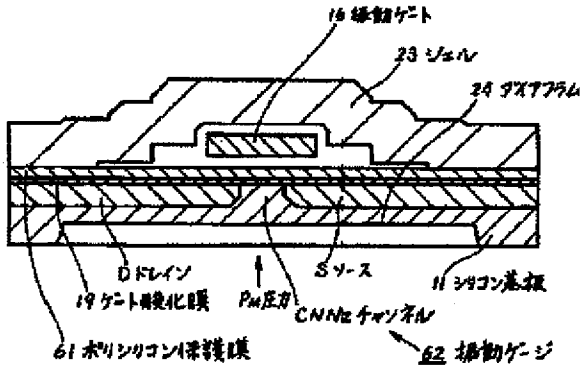
D Drain

E1 and E2 DC power supply

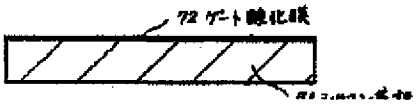
CNN1 and CNN2 Channel

DRAWINGS

[Drawing 1]



[Drawing 2]



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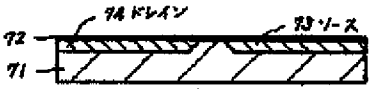

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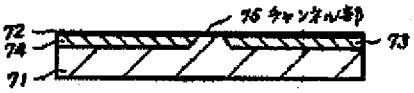

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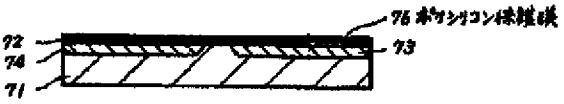

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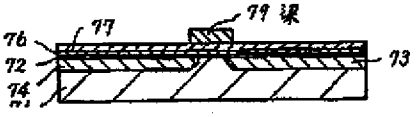

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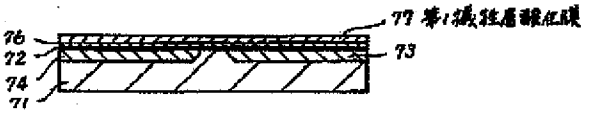
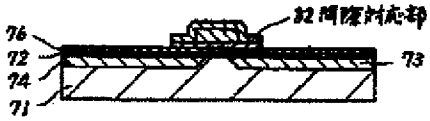
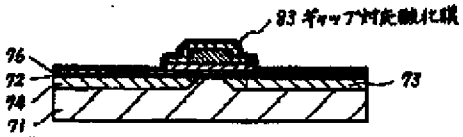


[Drawing 8]

[Drawing 9]



[Drawing 10]



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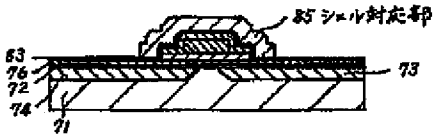

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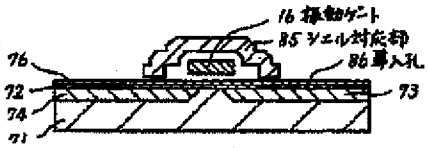
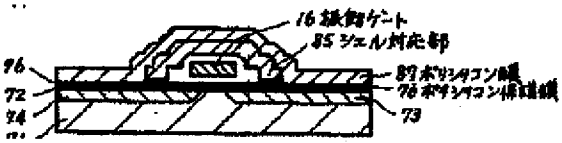
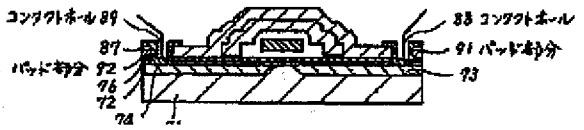


[Drawing 13]



[Drawing 14]



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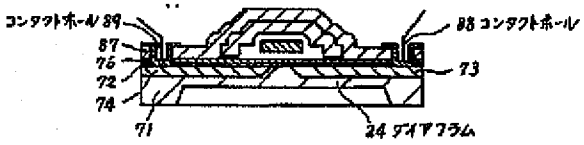

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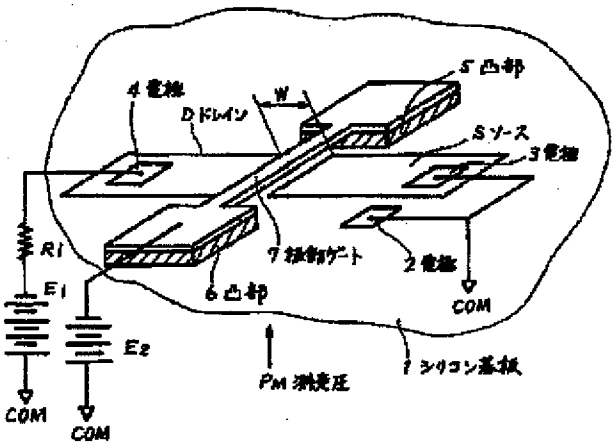
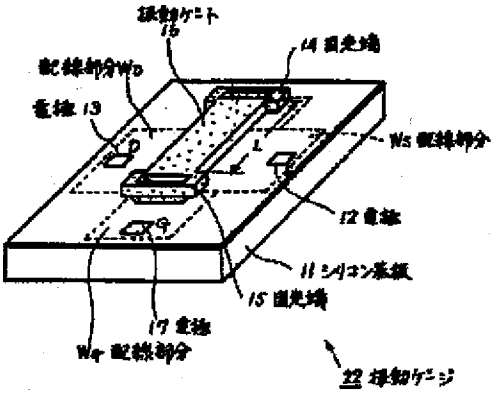


[Drawing 18]



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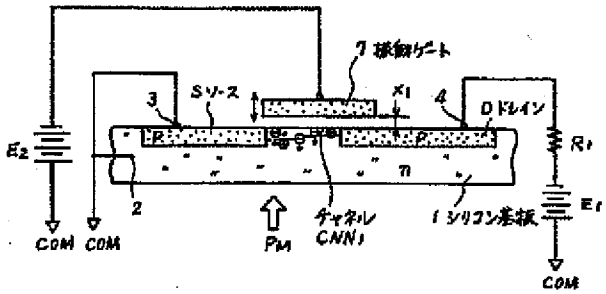

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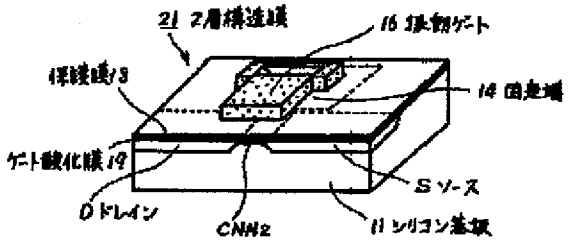
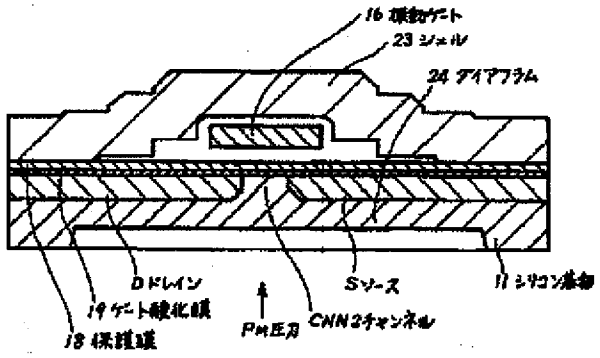
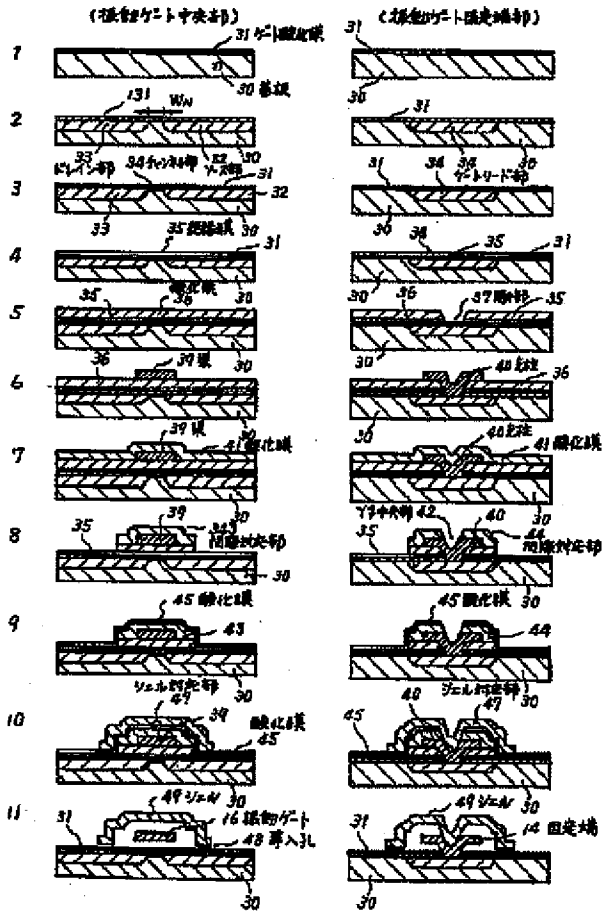


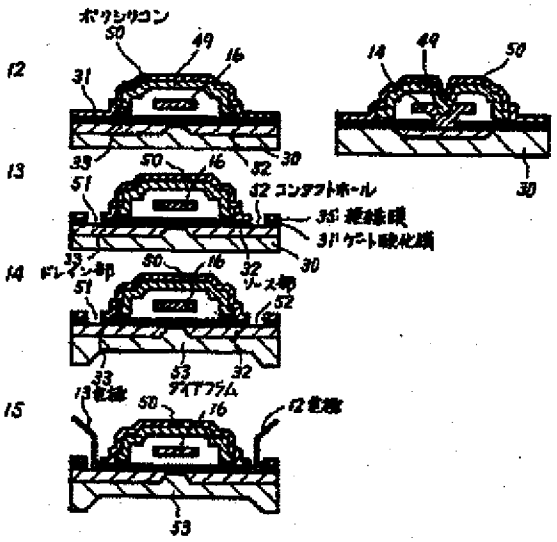
[Drawing 20]



[Drawing 21]



[Drawing 22]



Ref 2

対応なし、英抄

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9/00			9/00	Ｃ	
Ｈ０１Ｌ　29/78			Ｈ０１Ｌ　29/78	３０１Ｊ	

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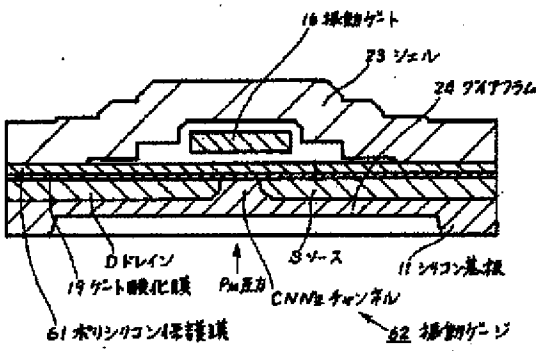
(54)【発明の名称】　振動式トランスデューサとその製造方法

(57)【要約】

【課題】　ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサとその製造方法を提供するにある。

【解決手段】　両端が基板に固定された振動ゲートの共振周波数を測定する事により振動ゲートの両端に加えられた歪を測定する振動式トランスデューサとその製造方法において、第１の伝導形式を有する半導体の基板と、基板の表面に形成され前記伝導形式とは逆の第２の伝導形式を有するドレインとソースにより挟まれたチャネルと、基板の表面上に形成されたゲート酸化膜と、ゲート酸化膜の上を覆うポリシリコン保護膜と、ポリシリコンよりなり変位可能なようにポリシリコン保護膜の表面から間隙を保持して両端が基板に固定されドレインとソースとチャネルとを覆って配置され自励発振によりドレインとの間に生じる静電力により変位する板状の導電性の振動ゲートとを具備したことを特徴とする振動式トランスデューサとその製造方法である。



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【特許請求の範囲】

【請求項１】両端が基板に固定された振動ゲートの共振周波数を測定する事により該振動ゲートの両端に加えられた歪を測定する振動式トランスデューサにおいて、

第１の伝導形式を有する半導体の基板と、

該基板の表面に形成され前記伝導形式とは逆の第２の伝導形式を有するドレインとソースにより挟まれたチャネルと、

前記基板の表面上に形成されたゲート酸化膜と、

該ゲート酸化膜の上を覆うポリシリコン保護膜と、

ポリシリコンよりなり変位可能なように該ポリシリコン保護膜の表面から間隙を保持して両端が前記基板に固定され前記ドレインとソースとチャネルとを覆って配置され自励発振により該ドレインとの間に生じる静電力により変位する板状の導電性の振動ゲートとを具備したことを特徴とする振動式トランスデューサ。

【請求項２】少なくとも１個所が前記半導体基板あるいは前記振動ゲートに電気的に接続されたポリシリコン保護膜を具備したことを特徴とする請求項１記載の振動式トランスデューサ。

【請求項３】前記チャネルに対向する前記ポリシリコン保護膜の部分に不純物が拡散されて形成された導通部を具備したことを特徴とする請求項１又は請求項２記載の振動式トランスデューサ。

【請求項４】前記振動ゲートを覆い内部が真空に保持されたシエルを具備したことを特徴とする請求項１又は請求項２又は請求項３記載の振動式トランスデューサ。

【請求項５】両端が基板に固定された振動ゲートの共振周波数を測定する事により該振動ゲートの両端に加えられた歪を測定する振動式トランスデューサの製造方法において、

以下の工程を有することを特徴とする振動式トランスデューサの製造方法。

（ａ）第１の伝導形式を有する半導体の基板上に、ゲート酸化膜を形成するゲート酸化膜形成工程。

（ｂ）第２の伝導形式となる不純物をソース、ドレインやゲートのリード部分に対応する所定領域にイオン注入するイオン注入工程。

（ｃ）前記ゲート酸化膜上にポリシリコン保護膜を成膜するポリシリコン保護膜形成工程。

（ｄ）該ポリシリコン保護膜上に第１犠牲層酸化膜を形成する第１犠牲層酸化膜形成工程。

（ｅ）該第１犠牲層酸化膜上にポリシリコン膜を成膜する。この後、導電性付与のため第２の伝導形式となる不純物をドープする。該ポリシリコン膜をエッチングして振動ゲートに対応する梁を形成する梁形成工程。

（ｆ）前記第１犠牲層酸化膜と前記梁の上に第２犠牲層酸化膜を形成する第２犠牲層酸化膜形成工程。

（ｇ）前記第１，第２犠牲層酸化膜をエッチングして間隙対応部を形成する間隙対応部形成工程。

2

（ｈ）犠牲層としてのギャップ対応酸化膜を前記ポリシリコン保護膜と間隙対応部の上を含んで全面に形成するギャップ対応膜形成工程。

（ｉ）該ギャップ対応酸化膜上にポリシリコン膜を成膜する。該ポリシリコン膜をエッチングしてシェル対応部を形成するシェル対応部形成工程。

（ｊ）前記ギャップ対応酸化膜をエッチングして導入孔を形成し、この導入孔を介して前記間隙対応部をも除去するエッチングギャップ形成工程。

（ｋ）真空中で前記シェル対応部、前記導入孔、前記ポリシリコン保護膜上を、ポリシリコン膜で成膜して、シェルの内部を真空に保持する真空封止工程。

（ｌ）前記ソース部と前記ドレイン部の上部にある前記ゲート酸化膜、前記ポリシリコン保護膜、及び前記ポリシリコン膜の一部をエッチング除去して開口しコンタクトホールを形成する。この後、該コンタクトホール部にパッド部分を形成し、金線でボンディングして配線を行なう電極形成工程。

（ｍ）前記第１の伝導形式を有する半導体の基板の底部をエッチングしてダイアフラムを形成するダイアフラム形成工程。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサとその製造方法に関するものである。

【０００２】

【従来の技術】図１６は従来より一般に使用されている従来例の原理的構成説明図で、振動式トランスデューサを圧力センサとして用いた例で、例えば、特開平７－３０１２８に示されている。

【０００３】シリコン基板１は、例えば、伝導形式がｎ形に形成され、ここには電極２が固定され、電極２は共通電位点ＣＯＭに接続されている。このシリコン基板１の上面には、ｐ形の不純物が拡散されてソースＳが形成され、ここにソースＳの電位を取り出すための電極３が形成されている。また、このシリコン基板１の下面には、測定すべき圧力P_xが印加される。

【０００４】また、このソースＳに対して所定間隔Ｗだけ離れて、同じくシリコン基板１の上面にｐ形の不純物が拡散されてドレインＤが形成され、ここにドレインＤの電位を取り出すための電極４が形成されている。

【０００５】シリコン基板１の所定間隔Ｗの部分の上方には、x_1だけ離れて凸部５、６が形成され、不純物が拡散されて導電性が付与された板状の振動子として機能する振動ゲート７（便宜的にＧなる符号を用いることもある）の両端が、これ等の凸部５、６に固定されている。

【０００６】つまり、振動ゲート７とシリコン基板１と

は両端を除いてx_1だけ離れて配置され、この振動ゲート7に対応するシリコン基板1には図示されていないがドレインDとソースSとの間にチャネルCNN1が形成される。

【0007】電極4と共通電位点COMとの間には、抵抗R1と直流電源E1とが直列に接続され、共通電位点COMに対して、ドレインDの電位は負電位に保持されている。また、振動ゲート7には直流電源E2が共通電位点COMに対して負電位になるように接続されている。

【0008】図17は図16の動作を説明する説明図である。振動ゲート7の長手方向から見たシリコン基板1の断面を含む構成となっている。ゲートとして機能する振動ゲート7には、直流電源E2から負の電位が印加されているので、図17に示すように電子は振動子7の下の表面からシリコン基板1の内部（図17では下の方）へ押しやられ、逆に正孔は表面に引き寄せられるようになる。

【0009】引き寄せられた正孔（P形）によって表面に細いP形の伝導層であるチャネルCNN1が形成されソースS（P形）とドレインD（P形）との間をP形で結ぶことになり、このためソースSとドレインDとの間に電流i_{d1}が流れる。

【0010】この電流i_{d1}によって発生するドレインDの電圧は、ドレイン抵抗R_Dと、ドレインとシリコン基板1との間に形成される静電容量C_Dにより、位相シフトを受け、この位相シフトを受けた電位変化により振動ゲート7とドレインDとの間の静電吸引力を変化させ間隔x_1を変化させる。

【0011】この間隔x_1の変化によりチャネルCNN1の厚さを変化させ、これにより電流i_{d1}を変化させ、これがドレインの電位変化を引き起こす。これを繰り返して発振するが、この発振はドレイン抵抗R_DとドレインDとシリコン基板1の間の静電容量C_Dと発振の発振角速度ωとの積（$\omega R_D C_D$）が1に比べて極めて大きくなる様に選定することにより継続される。

【0012】以上のように自励発振が維持されている状態で、図示のようにシリコン基板1に圧力P_Mが印加されると、振動ゲート7を固定する凸部5、6を介してこの圧力P_Mによる歪が振動ゲート7に加わり、これに対応して固有振動数が変化する。したがって、この固有振動数の変化を取り出すことにより、圧力P_Mの値を検知することができる。

【0013】図18は、図16の具体的実施例の構成を示す斜視図、図19はその中央部近傍の断面図である。ただし、振動ゲートを覆うシエル部分とダイアフラム部分については省略してある。図20は振動ゲートの中央部分における全体側断面図である。

【0014】図18、図19、図20において、シリコン基板11は、例えば伝導形式がn形に形成され、このシリコン基板11の上面には、p形の不純物が拡散されてソースSが形成され、ここにソースSの電位を取り出すためのアルミニウム製の電極12が、点線で示す配線部W_Sを介して形成されている。また、このシリコン基板11の下面には図示していないがダイアフラムが凹部状に形成されここに測定すべき圧力P_Mが印加される。

【0015】また、このソースSに対して所定間隔だけ離れて、同じくシリコン基板11の上面にp形の不純物が拡散されてドレインDが形成され、ここにドレインDの電位を取り出すためのアルミニウム製の電極13が点線で示す配線部W_Dを介して形成されている。

【0016】シリコン基板11の上方には、間隙x_2だけ離れて固定端14、15が形成され、不純物が拡散されて導電性が付与されたポリシリコンの板状の振動ゲート16の両端が、これ等の固定端14、15に一体に固定されている。振動ゲート16の梁の長さはLである。そして、この振動ゲート16はアルミニウム製の電極17と点線で示す配線部分W_Gを介して接続されている。

【0017】つまり、振動ゲート16とシリコン基板11とは両端を除いて間隙x_2だけ離れて配置され、この振動ゲート16に対応するシリコン基板11のドレインDとソースSとの間にチャネルCNN2が形成される。

【0018】シリコン基板11の上面に形成されたこれらのドレインD、チャネルCNN2およびソースSの上には弗化水素酸（HF）に対する耐食性の高い保護膜18、例えばSi_3N_4、$Si_xC_yN_w$、Si_xC、Al_2O_3などと、酸化膜19とからなる2層構造膜21が形成されている。保護膜18は酸化膜19と同様な絶縁体である。

【0019】そして、この2層構造膜21と振動ゲート16との間は、振動ゲート16が固定端14、15を節として上下に振動できるように間隙が設けられている。このようにして振動ゲージ22が構成されている。23はシエル、24はダイアフラムである。

【0020】今までの説明では、図18に示すような振動ゲージと電子回路とを結合して振動式トランスデューサを構成する点について説明した。次に、このような振動式トランスデューサの構成要素としての振動ゲージ22を製造する製造方法について、図21と図22に示す製造工程図を用いて説明する。

【0021】なお、図22に示す製造工程は、図21に示す製造工程に連続して続くものであるが、説明の便宜上2つに分割してある。図18に示す構成では、振動ゲート16の部分とこれを両端で固定する固定端14、15の部分とでは製造工程の過程で生じる断面構造が異なるので、同一工程ではあるが左右に分離してこれらを各別に図示する。

【0022】左側の図は振動ゲート16の中央部の断面構造で、右側の図が固定端14の部分の断面構造である。なお、固定端15の部分は固定端14の部分と同一の構造であるので省略する。

【００２３】ステップ１は、ゲート酸化膜形成工程を示す。ｎ形のシリコン単結晶の基板３０の上にゲート酸化膜３１を、例えば５００オングストローム程度の厚さに形成する。この工程では、振動ゲートの中央部と固定端部での断面構造は同一に形成される。この後、ステップ２に移行する。以後、各ステップをステップ番号に従って進行する。

【００２４】ステップ２は、イオン注入工程を示す。ここでは、ｐ形不純物としてボロンを所定領域にイオン注入する。これにより、振動ゲートの中央部ではチャネルＣＣＮを形成する予定の所定間隔W_nをおいてｐ形のソース部３２（図１８のW_sに対応）とドレイン部３３（図１８のW_Dに対応）とを形成し、固定端部ではｐ形のゲートリード部３４（図１８のW_cに対応）を形成する。

【００２５】ステップ３は、チャネル形成工程を示す。ここでは、振動ゲートの中央部においてチャネルＣＣＮを形成する予定の所定間隔W_nのチャネル部３４（ＣＣＮ２）にボロンを浅い深さでイオン注入する。これによって、ソース・ドレイン間の抵抗を所定値に制御することができる。この場合、固定端部では変化がない。

【００２６】ステップ４は、窒化膜形成工程を示す。この工程では、後工程で使用する弗化水素酸（ＨＦ）に対する、ゲート酸化膜３１の保護のために、弗化水素酸に対して耐性が強い絶縁膜３５として、例えば$Si_xC_yN_z$膜を、ほぼ１０００オングストローム程度の厚さで、ゲート酸化膜３１の上に成膜する。

【００２７】ステップ５は、第１犠牲層酸化膜形成工程を示す。この工程は、先ず、最終的に振動ゲート１６の周囲に空隙を形成するための下側の犠牲層としてＣＶＤ（Chemical Vapour Deposition）法により５０００オングストローム程度の厚さに絶縁膜３５の上に酸化膜３６を形成する。

【００２８】次に、固定端部に対しては、フオトリソグラフイ技術により固定端１４が形成される予定の部分のゲート酸化膜３１、絶縁膜３５、及び酸化膜３６の部分を開口部３７として開口する。

【００２９】ステップ６は、ポリシリコン成膜工程を示す。この工程は最終的に振動ゲート１６と固定端１４とを形成するための前工程である。先ず、酸化膜３６と開口部３７の上にポリシリコン３８を例えば１μｍ程度の厚さで成膜する。この後、導電性を付与するためにボロンをドープする。

【００３０】次に、フオトリソグラフイ技術により振動ゲート１６に対応する部分と開口部３７に対応する部分にマスクをしてから、ＲＩＥ（Reactive Ion Etching）によりポリシリコン３８を所定の形状にエッチングして最終的に振動ゲートとなる板状の梁３９と、開口部３７にＹ形の支柱４０を形成する。

【００３１】ステップ７は、第２犠牲層酸化膜形成工程

を示す。この工程は、最終的に振動ゲート１６の周囲に空隙を形成するための、下側を除く部分の犠牲層としてＣＶＤ法により５０００オングストローム程度の厚さに酸化膜３６、梁３９、及び支柱４０の上に酸化膜４１を形成する。

【００３２】ステップ８は、酸化膜エッチング工程を示す。まず、フオトリソグラフイ技術により振動ゲートの中央部では梁３９の近傍を、固定端部では支柱４０の近傍と支柱４０のＹ字中央部４２を除く部分をマスクしてから、これらの周囲の酸化膜３６と４１を弗化水素酸でエッチングして間隙対応部４３、４４を形成する。

【００３３】ステップ９は、ギャップ対応成膜工程を示す。この工程は、後工程で用いられるエッチング液を導入するための犠牲層としての酸化膜４５を、ほぼ５００オングストローム程度の厚さで絶縁膜３５と間隙対応部４３、４４の上を含んで全面にＣＶＤ法により形成する。この後、フオトリソグラフイ技術を用いてＹ字中央部４２の上の酸化膜４５をエッチングして除去する。

【００３４】ステップ１０は、シエル対応部形成工程を示す。ステップ９で形成された酸化膜４５などの上に１μｍ程度の厚さになるようにポリシリコン４６を成膜する。この後、ＲＴＡ（Rapid Thermal Aneal）によりシエル及び振動ゲートのポリシリコンに残存するストレスを短時間熱処理して除去し、これらが変形するのを防止する。

【００３５】この後、フオトリソグラフイ技術を用いてマスクし、ＲＩＥによりポリシリコン４６をエッチングして振動ゲートを覆う大きさの範囲にシエル対応部４７を形成する。

【００３６】ステップ１１は、エッチングギャップ形成工程を示す。この工程は、振動ゲートとシエルとを形成するために、弗化水素酸を用いて酸化膜４５をエッチングしながらこれを除去して導入孔４８を形成し、ついでこの導入孔４８を介して間隙対応部４３、４４をも除去する。このようにして、振動ゲート１６、固定端１４、及びシエル４９を形成する。

【００３７】ステップ１２は、真空封止工程を示す。この工程は、真空中でシエル４９、導入孔４８、絶縁膜３５の上をポリシリコン５０でほぼ５０００オングストローム程度の厚さで成膜して、シエル４９の内部を真空に保持する。

【００３８】ステップ１３は、コンタクトホール形成工程を示す。ソース部３２とドレイン部３３の上部にあるゲート酸化膜３１、絶縁膜３５、及びポリシリコン５０の一部をフオトリソグラフイ技術とＲＩＥとを用いて開口してコンタクトホール５１、５２を形成する。同様にして、ゲート部にもコンタクトホール５４を形成することができる。

【００３９】ステップ１４は、ダイアフラム形成工程を示す。水酸化カリウム（ＫＯＨ）液を用いて、中央部が

薄肉で周囲が厚肉となる薄肉部になるようにシリコン単結晶の基板３０の底部をエッチングしてダイアフラム５３を形成する。

【００４０】ステップ１５は、ボンデング工程を示す。コンタクトホール５１、５２にアルミニウム製の電極１３、１２を形成する。以上が、振動式トランスデューサの振動ゲージをシェルで覆いダイアフラムを形成する製造方法である。

【００４１】

【発明が解決しようとする課題】しかしながら、この様な、微細加工技術（マイクロマシーニング）を用いて、半導体基板上に形成された構造型トランスデューサにおいては、以下のような問題がある。

【００４２】１）振動ゲート１６などの構造物を作製する工程で、犠牲層にシリコン酸化膜３６，４１を用いるため、これを除去する工程で、弗化水素酸で長時間エッチングする必要がある。このとき、シリコン基板１１側に設けられ、絶縁膜として必要なゲート酸化膜１９など、エッチングされて欲しくない膜は、ゲート酸化膜１９と同様な絶縁物であるシリコン窒化膜１８等の、耐弗化水素酸性の高い保護膜１８で保護しておく必要があるが、十分な耐蝕性は得られていなかった。

【００４３】２）更に、ゲート酸化膜１９をシリコン窒素化膜などの耐弗化水素酸性の高い保護膜で保護すると、シリコン窒化膜１８等の膜により、ゲート酸化膜１９との界面に準位が出来るために、ＦＥＴに相当する部分のしきい値電圧の絶対値が大きくなり、オンしずらくなったり、バラツキが大きくなる。この界面の準位は不安定なため、ドリフトなどの電気的特性の劣化を引き起こす。

【００４４】また、この構造では、通常のＭＯＳＦＥＴのゲートに相当する電極部分が、絶縁膜に接していないため、絶縁膜中に水平方向に、電位勾配が発生してソース近傍での電位が低下し、そのためにしきい値電圧を押し上げる結果になっている。

【００４５】このため、動作点を一定にした時に、ドレイン電流の大きさに、ばらつきがでたり、ドリフトが生じたりする問題があった。

３）また、製作工程中、または、完成後の動作中に、振動ゲート１６がシリコン基板１１に付着してしまうという問題があり、余り剛性の小さい梁構造を作製することができなかった。

【００４６】しかし、梁構造を有する高感度の振動式センサを作製しようとする場合、大きな周波数変化率を得ようとすると、梁の長さを長く、厚さを薄くしなければならないが、このような梁は剛性が小さく、容易にシリコン基板に付着してしまうため、高感度な振動式センサを作製する事は困難であった。

【００４７】以上のような問題点に対して、以下の解決方法を採用した。

１）ポリシリコン膜は、弗化水素酸水溶液に対する耐蝕性は、シリコン窒化膜１８等に比較して十分に強く、犠牲層のシリコン酸化膜３６，４１を除去して構造物を形成するのに、十分な耐蝕性を備えている。

【００４８】２）ドリフト等電気特性の不安定性の原因は、主として絶縁膜１８と酸化膜１９のあいだの界面準位であると考えられる。そこで、絶縁膜１８の替りに、酸化膜１９との界面状態が安定で、弗化水素酸に強い耐性を持つポリシリコン膜を用いると、従来並みの特性に加え、ドリフトがほとんどなくなり、しきい値電圧のばらつきも少なくすることができた。

【００４９】更に加えるに、ポリシリコン膜のチャネル部分に、ボロン又はリン等の不純物を導入すると、しきい値は小さく安定化することが出来る。

【００５０】２）付着の原因としては主として以下の２つがある。

❶振動ゲート１６と基板１１とが接触した時に働く、分子(あるいは原子)間吸引力。

❷絶縁体１９に、摩擦などの原因で電荷が注入されることによって、絶縁体１９が帯びる静電気。

【００５１】これらを解決する方法として、以下のような対策を行なった。❶については、付着現象と基板１１の表面荒さの関係を調べ、表面荒さが大きければ付着が起きにくいことを利用して解決を行なった。

【００５２】❷については、基板１１あるいは振動ゲート１６に少なくとも１個所を接続された、半絶縁性のポリシリコン膜で、基板１１の表面を覆うことによって解決した。

【００５３】本発明の目的は、ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサとその製造方法を提供するにある。

【００５４】

【課題を解決するための手段】この目的を達成するために、本発明は、

（１）両端が基板に固定された振動ゲートの共振周波数を測定する事により該振動ゲートの両端に加えられた歪を測定する振動式トランスデューサにおいて、第１の伝導形式を有する半導体の基板と、該基板の表面に形成され前記伝導形式とは逆の第２の伝導形式を有するドレインとソースにより挟まれたチャネルと、前記基板の表面上に形成されたゲート酸化膜と、該ゲート酸化膜の上を覆うポリシリコン保護膜と、ポリシリコンよりなり変位可能なように該ポリシリコン保護膜の表面から間隙を保持して両端が前記基板に固定され前記ドレインとソースとチャネルとを覆って配置され自励発振により該ドレインとの間に生じる静電力により変位する板状の導電性の振動ゲートとを具備したことを特徴とする振動式トランスデューサ。

（２）少なくとも１個所が前記半導体基板あるいは前記

振動ゲートに電気的に接続されたポリシリコン保護膜を具備したことを特徴とする請求項1記載の振動式トランスデューサ。

（3）前記チャネルに対向する前記ポリシリコン保護膜の部分に不純物が拡散されて形成された導通部を具備したことを特徴とする請求項1又は請求項2記載の振動式トランスデューサ。

（4）前記振動ゲートを覆い内部が真空に保持されたシェルを具備したことを特徴とする請求項1又は請求項2又は請求項3記載の振動式トランスデューサ。

（5）両端が基板に固定された振動ゲートの共振周波数を測定する事により該振動ゲートの両端に加えられた歪を測定する振動式トランスデューサの製造方法において、以下の工程を有することを特徴とする振動式トランスデューサの製造方法。

（a）第1の伝導形式を有する半導体の基板上に、ゲート酸化膜を形成するゲート酸化膜形成工程。

（b）第2の伝導形式となる不純物をソース、ドレインやゲートのリード部分に対応する所定領域にイオン注入するイオン注入工程。

（c）前記ゲート酸化膜上にポリシリコン保護膜を成膜するポリシリコン保護膜形成工程。

（d）該ポリシリコン保護膜上に第1犠牲層酸化膜を形成する第1犠牲層酸化膜形成工程。

（e）該第1犠牲層酸化膜上にポリシリコン膜を成膜する。この後、導電性付与のため第2の伝導形式となる不純物をドープする。該ポリシリコン膜をエッチングして振動ゲートに対応する梁を形成する梁形成工程。

（f）前記第1犠牲層酸化膜と前記梁の上に第2犠牲層酸化膜を形成する第2犠牲層酸化膜形成工程。

（g）前記第1，第2犠牲層酸化膜をエッチングして間隙対応部を形成する間隙対応部形成工程。

（h）犠牲層としてのギャップ対応酸化膜を前記ポリシリコン保護膜と間隙対応部の上を含んで全面に形成するギャップ対応膜形成工程。

（i）該ギャップ対応酸化膜上にポリシリコン膜を成膜する。該ポリシリコン膜をエッチングしてシェル対応部を形成するシェル対応部形成工程。

（j）前記ギャップ対応酸化膜をエッチングして導入孔を形成し、この導入孔を介して前記間隙対応部をも除去するエッチングギャップ形成工程。

（k）真空中で前記シェル対応部、前記導入孔、前記ポリシリコン保護膜上を、ポリシリコン膜で成膜して、シェルの内部を真空に保持する真空封止工程。

（l）前記ソース部と前記ドレイン部の上部にある前記ゲート酸化膜、前記ポリシリコン保護膜、及び前記ポリシリコン膜の一部をエッチング除去して開口しコンタクトホールを形成する。この後、該コンタクトホール部にパッド部分を形成し、金線でボンディングして配線を行なう電極形成工程。

（m）前記第1の伝導形式を有する半導体の基板の底部をエッチングしてダイアフラムを形成するダイアフラム形成工程。

【0055】

【発明の実施の形態】図1は本発明の一実施例の要部構成説明図である。図において、図20と同一記号の構成は同一機能を表わす。以下、図20と相違部分のみ説明する。61は、ゲート酸化膜19の上を覆うポリシリコン保護膜である。

【0056】以上の構成において、ゲートとして機能する振動ゲート16には、直流電源E2から負の電位が印加されているので、電子は振動ゲート16の下の表面からシリコン基板11の内部へ押しやられ、逆に正孔は表面に引き寄せられるようになる。

【0057】引き寄せられた正孔（P形）によって表面に細いP形の伝導層であるチャネルCNN2が形成されソースS（P形）とドレインD（P形）との間をP形で結ぶことになり、このためソースSとドレインDとの間に電流i_{d2}が流れる。

【0058】この電流i_{d2}によって発生するドレインDの電圧は、ドレイン抵抗R_Dと、ドレインとシリコン基板11との間に形成される静電容量C_Dにより、位相シフトを受け、この位相シフトを受けた電位変化により振動ゲート16とドレインDとの間の静電吸引力を変化させ間隔x_2を変化させる。

【0059】この間隔x_2の変化によりチャネルCNN2の厚さを変化させ、これにより電流i_{d2}を変化させ、これがドレインの電位変化を引き起こす。これを繰り返して発振するが、この発振はドレイン抵抗R_DとドレインDとシリコン基板11の間の静電容量C_Dと発振の発振角速度ωとの積（$\omega R_D C_D$）が1に比べて極めて大きくなる様に選定することにより継続される。

【0060】以上のように自励発振が維持されている状態で、シリコン基板11に圧力P_aが印加されると、振動ゲート16を固定する固定端14，15を介して、この圧力P_aによる歪が振動ゲート16に加わり、これに対応して固有振動数が変化する。したがって、この固有振動数の変化を取り出すことにより、圧力P_aの値を検知することができる。

【0061】この結果、

（1）基板11構造の最表面に形成されたポリシリコン保護膜61は、弗化水素酸水溶液の耐蝕性が充分であり、振動ゲート16の製造工程中において、犠牲層エッチング時に、ゲート酸化膜19が弗化水素酸水溶液にさらされて、素子構造が破壊されることがない。

【0062】（2）ポリシリコン保護膜61は、ゲート酸化膜19との界面状態が良好に出来るため、しきい値のばらつきを押さえ、ドリフトが殆ど発生しない等、電気的な安定性が得られる振動式トランスデューサが得られる。

【0063】（3）ポリシリコン保護膜61は、膜厚を厚く成長させると、表面に微小な凸凹が出来、表面粗さを変える事ができる。この表面粗さと付着の関係を実験により調べた結果、ポリシリコン保護膜61を用いることにより、表面付着エネルギーを下げ、振動ゲート16が付着しにくくすることができた。

【0064】また、振動ゲート16等のシリコンの構造体を、犠牲層エッチングで切り離す前の工程で、既に、ポリシリコン保護膜61が形成されているため、切り離しの犠牲層エッチング工程で、シリコン基板11に振動ゲート16が付着することを防止する事ができる。

【0065】更に、この構造では、犠牲層エッチング導入孔86を狭くできるため、真空封止工程で、真空封止のためのポリシリコン87が、振動ゲート16の外周面に付着し、振動ゲート16の残留引張り歪を緩和したり、断面形状が太く変化したりすることがなく、振動ゲート16の共振周波数のばらつきを小さく抑える事ができる。

【0066】次に、少なくとも1個所が半導体基板11、あるいは振動ゲート16に電気的に接続された半絶縁性のポリシリコン膜保護膜61で、基板11の表面を覆うようにすれば、静電気等の要因により、ゲート酸化膜19に電荷が注入されても、電荷の帯電を抑え、静電気による振動ゲート16の、基板11やシェル23の壁面への付着を防止できる振動式トランスデューサを得る事ができる。

【0067】次に、チャネルCNN2に対向するポリシリコン保護膜61の部分に、不純物が拡散されて形成された導通部が設けられれば、しきい値は小さく安定化することができる振動式トランスデューサが得られる。

【0068】また、振動ゲート16を覆い、内部が真空に保持されたシェル23が設けられれば、振動ゲート16の振動のQ値を高くすることができ、高精度な振動式トランスデューサを得ることができる。

【0069】次に、このような振動式トランスデューサの構成要素としての振動ゲージ22を製造する製造方法について、図2から図15に示す製造工程図を用いて説明する。

【0070】（1）図2は、ゲート酸化膜形成工程を示す。n形のシリコン単結晶の基板71の上に、ゲート酸化膜72を、例えば500オングストローム程度の厚さに形成する。

【0071】（2）図3は、イオン注入工程を示す。ここでは、p形不純物としてボロンを、ソース73、ドレイン74やゲートのリード部分に対応する所定領域に、イオン注入しする。

【0072】（3）図4は、また、必要に応じて、チャネル部75に、ボロンを浅い深さでイオン注入することで、ソース73－ドレイン74間の抵抗値を制御することが可能である。

【0073】（4）図5は、ポリシリコン保護膜形成工程を示す。この工程では、後工程で使用する弗化水素酸（HF）に対して耐性が強く、ゲート酸化膜72の保護膜の役目を果たし、かつ安定な膜であるポリシリコン保護膜76を、ほぼ5000オングストローム程度の厚さでゲート酸化膜72の上に成膜する。

【0074】（5）図6は、第1犠牲層酸化膜形成工程を示す。この工程は、先ず、最終的に振動ゲートの周囲に空隙を形成するための下側の犠牲層として例えばCVD（Chemical Vapor Deposition）法により5000オングストローム程度の厚さにポリシリコン保護膜76の上に第1犠牲層酸化膜77を形成する。

【0075】（6）図7は、梁形成工程を示す。この工程は最終的に振動ゲート16を形成するための前工程である。先ず、第1犠牲層酸化膜77の上に、ポリシリコン膜78（図示せず）を、例えば1μm程度の厚さで成膜する。この後、導電性を付与するためにボロンをドープする。

【0076】次に、フオトリソグラフイ技術により、振動ゲート16に対応する部分に、マスクをしてから、RIE（Reactive Ion Etching）により、ポリシリコン78（図示せず）を所定の形状にエッチングして、最終的に振動ゲート16となる板状の梁79を形成する。

【0077】（7）図8は、第2犠牲層酸化膜形成工程を示す。この工程は、先ず、最終的に振動ゲート16の周囲に空隙を形成するための、下側を除く部分の犠牲層として、例えばCVD法により、5000オングストローム程度の厚さに、第1犠牲層酸化膜77と梁79の上に、第2犠牲層酸化膜81を形成する。

【0078】（8）図9は、間隙対応部形成工程を示す。先ず、フォトリソグラフィ技術により、振動ゲート16の中央部では梁79の近傍をマスクしてから、これらの周囲の第1犠牲層酸化膜77と第2犠牲層酸化膜81を、弗化水素酸でエッチングして、間隙対応部82を形成する。

【0079】（9）図10は、ギャップ対応膜形成工程を示す。この工程は、後工程で用いられる、エッチング液を導入するための犠牲層としてのギャップ対応酸化膜83を、ほぼ500オングストローム程度の厚さで、ポリシリコン保護膜76と間隙対応部82の上を含んで全面にCVD法により形成する。

【0080】（10）図11は、シェル対応部形成工程を示す。図10で形成されたギャップ対応酸化膜83上に、1μm程度の厚さになるようにポリシリコン膜84（図示せず）を成膜する。

【0081】この後、フォトリソグラフィ技術を用いてマスクし、RIEによりポリシリコン膜84をエッチングして、振動ゲート16を覆う大きさの範囲に、シェル対応部85を形成する。

【0082】（11）図12は、エッチングギャップ形

成工程を示す。この工程は、振動ゲート１６とシェル対応部８５を形成するために、弗化水素酸を用いて，ギャップ対応酸化膜８３をエッチングしながら、これを除去して導入孔８６を形成し、ついでこの導入孔８６を介して間隙対応部８２をも除去する。このようにして、振動ゲート１６及びシェル対応部８５を形成する。

【００８３】（１２）図１３は、真空封止工程を示す。この工程は、真空中でシェル対応部８５、導入孔８６、ポリシリコン保護膜７６の上を、ポリシリコン膜８７でほぼ１μｍ程度の厚さで成膜して、シェル２３の内部を真空に保持する。

【００８４】（１３）図１４は、電極を形成する工程を示す。ソース部７３とドレイン部７４の上部にあるゲート酸化膜７２、ポリシリコン保護膜７６、及びポリシリコン膜８７の一部を、フォトリソグラフィ技術とＲＩＥとを用いて開口して、コンタクトホール８８，８９を形成する。

【００８５】この後、コンタクトホール８８，８９に、アルミニウムをスパッタリング法によって成膜し、フォトグラフィ技術を用いてパッド部分９１，９２を形成する。金線でボンディングして配線を行なう。

【００８６】（１４）図１５は、ダイアフラム形成工程を示す。水酸化カリウム（ＫＯＨ）液を用いて、中央部が薄肉で周囲が厚肉となる薄肉部になるように、シリコン単結晶の基板７１の底部をエッチングして、ダイアフラム２４を形成する。

【００８７】以上が、振動式トランスデューサの振動ゲージ６２を、シェル２３で覆い、ダイアフラム２４を形成する製造方法である．

【００８８】以上の様な本発明の製造方法によれば、ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサを、従来の半導体プロセスを利用して安価に且つ確実に製作出来る振動式トランスデューサの製造方法を得ることができる。

【００８９】

【発明の効果】以上、実施例と共に詳細に説明したように、本発明の第１請求項によれば、

（１）基板構造の最表面に形成されたポリシリコン保護膜は、弗化水素酸水溶液の耐蝕性が充分であり、振動ゲートの製造工程中において、犠牲層エッチング時に、ゲート酸化膜が弗化水素酸水溶液にさらされて素子構造が破壊されることがない。

【００９０】（２）ポリシリコン保護膜は、ゲート酸化膜との界面状態が良好に出来るため、しきい値のばらつきを押さえ、ドリフトが殆ど発生しない等、電気的な安定性が得られる振動式トランスデューサが得られる。

【００９１】（３）ポリシリコン保護膜は、膜厚を厚く成長させると、表面に微小な凸凹ができ、表面粗さを変える事ができる。この表面粗さと付着の関係を実験により調べた結果、ポリシリコン保護膜を用いることにより、表面付着エネルギーを下げ、振動ゲートが付着しなくすることができた。

【００９２】また、振動ゲート等のシリコンの構造体を、犠牲層エッチングで切り離す前の工程で、既に、ポリシリコン保護膜が形成されているため、切り離しの犠牲層エッチング工程で、シリコン基板に振動ゲートが付着することを防止する事ができる。

【００９３】更に、この構造では、犠牲層エッチング導入孔を狭くできるため、真空封止工程で、真空封止のためのポリシリコンが、振動ゲートの外周面に付着し、振動ゲートの残留引張り歪を緩和したり、断面形状が太く変化したりすることがなく，振動ゲートの共振周波数のばらつきを小さく抑える事ができる。

【００９４】本発明の第２請求項によれば、静電気等の要因により、ゲート酸化膜に電荷が注入されても、少なくとも１個所が半導体基板、あるいは、振動ゲートに電気的に接続された半絶縁性のポリシリコン膜保護膜で、ゲート酸化膜表面を覆う事によって、電荷の帯電を抑え、静電気による振動ゲートの、基板やシェル壁面への付着を防止できる振動式トランスデューサを得る事ができる。

【００９５】本発明の第３請求項によれば、チャネルに対向するポリシリコン膜の部分に、不純物が拡散されて形成された導通部が設けられたので、しきい値は小さく安定化することができる振動式トランスデューサが得られる。

【００９６】本発明の第４請求項によれば、振動ゲートを覆い内部が真空に保持されたシエルが設けられたので、振動ゲートの振動のＱ値を高くすることができ、高精度な振動式トランスデューサを得ることができる。

【００９７】本発明の第５請求項によれば、ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサを従来の半導体プロセスを利用して安価に且つ確実に製作出来る振動式トランスデューサの製造方法を得ることができる。

【００９８】従って、本発明によれば、ゲート絶縁膜が保護され、ドリフトが防止出来、振動ゲートの付着を防止し得る振動式トランスデューサとその製造方法を実現することが出来る。

【図面の簡単な説明】

【図１】本発明の１実施例の要部構成説明図である。

【図２】図１のゲート酸化膜形成工程説明図である。

【図３】図１のイオン注入工程説明図である。

【図４】図１のイオン注入工程説明図である。

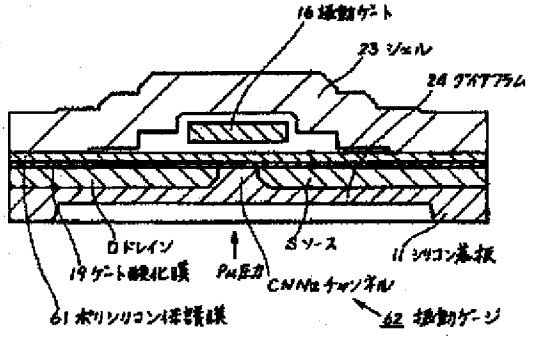
【図５】図１のポリシリコン保護膜形成工程説明図である。

【図６】図１の第１犠牲層酸化膜形成工程説明図である。

【図７】図１の梁形成工程説明図である。

【図８】図１の第２犠牲層酸化膜形成工程説明図である。
【図９】図１の間隙対応部形成工程説明図である。
【図１０】図１のギャップ対応膜形成工程説明図である。
【図１１】図１のシェル対応部形成工程説明図である。
【図１２】図１のエッチングギャップ形成工程説明図である。
【図１３】図１の真空封止工程説明図である。
【図１４】図１の電極形成工程説明図である。
【図１５】図１のダイアフラム形成工程説明図である。
【図１６】従来より一般に使用されている従来例の原理的構成説明図である。
【図１７】図１６の動作説明図である。
【図１８】図１６の具体的実施例の構成を示す斜視図である。
【図１９】図１８の中央部近傍の断面図である。
【図２０】図１８の振動ゲート１６の中央部分における全体側断面図である。
【図２１】図１８の製造工程説明図である。
【図２２】図１８の製造工程説明図である。
【符号の説明】
１１　シリコン基板
１２　電極
１３　電極
１４　固定端
１５　固定端
１６　振動ゲート
１７　電極
１９　ゲート酸化膜
＊２１　２層構造膜
２２　振動ゲージ
２３　シェル
２４　ダイアフラム
６１　ポリシリコン保護膜
７１　シリコン基板
７２　ゲート酸化膜
７３　ソース
７４　ドレイン
７５　チャネル部
７６　ポリシリコン保護膜
７７　第１犠牲層酸化膜
７８　ポリシリコン
７９　梁
８１　第２犠牲層酸化膜
８２　間隙対応部
８３　ギャップ対応酸化膜
８４　ポリシリコン膜
８５　シェル対応部
８６　導入孔
８７　ポリシリコン膜
８８　コンタクトホール
８９　コンタクトホール
９１　パッド部分
９２　パッド部分
Ｓ　ソース
Ｄ　ドレイン
Ｅ１、Ｅ２　直流電源
ＣＮＮ１、ＣＮＮ２　チャネル

【図１】



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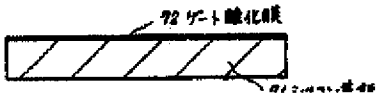

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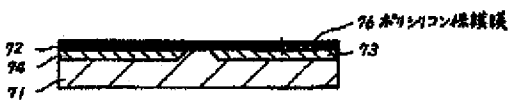

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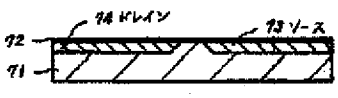

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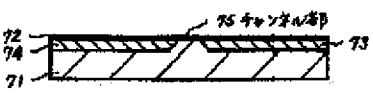

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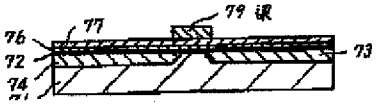

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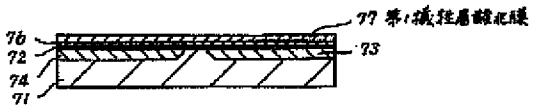

【図８】

【図９】

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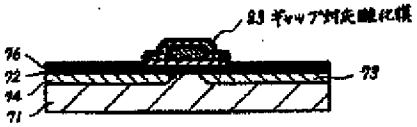

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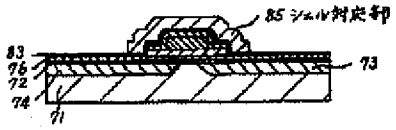

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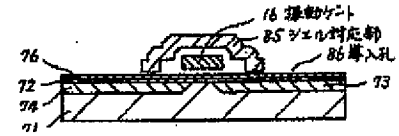

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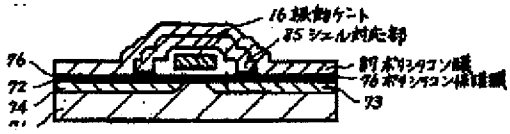
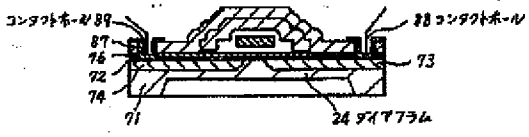


【図１４】

【図１５】



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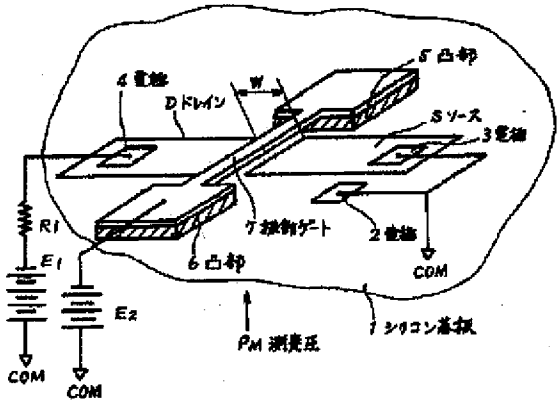

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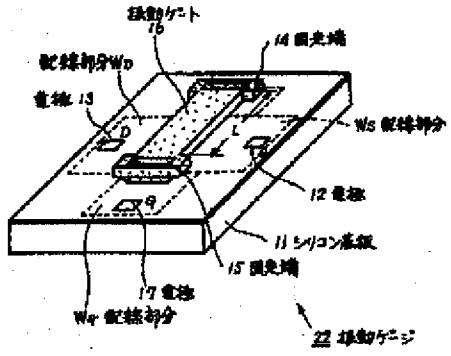

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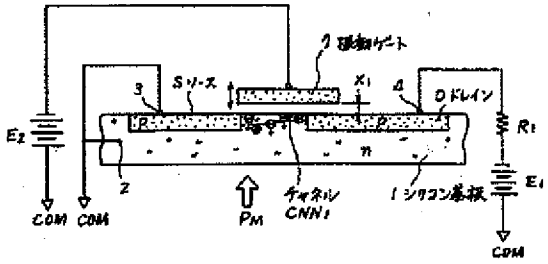

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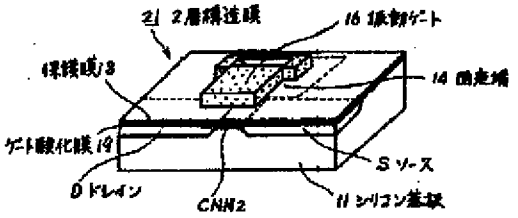

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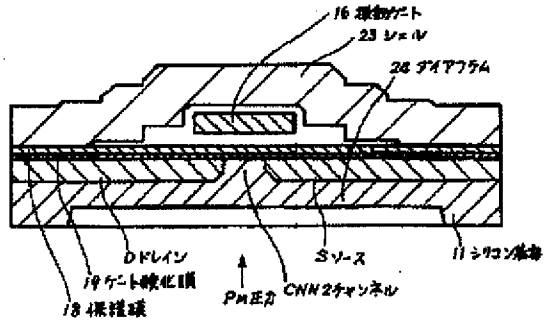

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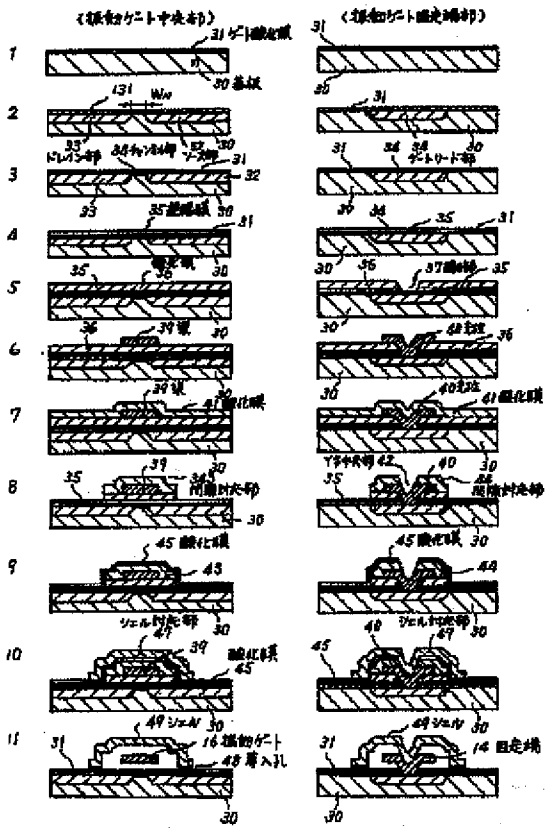

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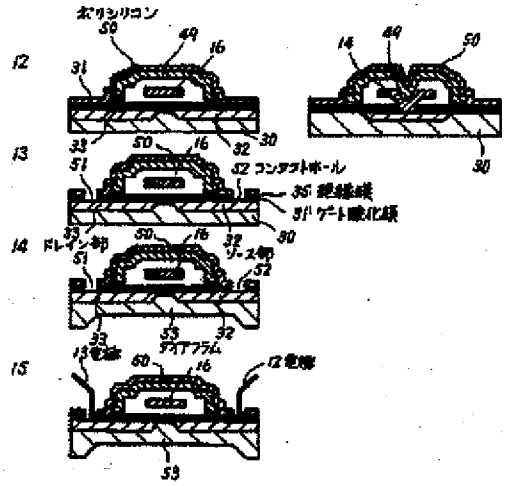

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(71)Applicant : YOKOGAWA ELECTRIC CORP

(72)Inventor : YOSHIDA TAKASHI
MIYAZAKI SHUNICHI

(54) OSCILLATORY TRANSDUCER AND FABRICATION THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent adhesion of an oscillatory gate by covering a gate oxide with polysilicon and providing a planar conductive oscillatory gate which is displaced by an electrostatic power generated with respect to a drain through self-oscillation thereby protecting a gate insulator and preventing drift.

SOLUTION: A gate oxide 72 is deposited on a substrate 71 and a stable polysilicon protective layer 76 resistant to hydrofluoric acid is formed thereon. A first sacrificial layer oxide film is then deposited on the polysilicon protective layer 76 and a polysilicon is deposited thereon and doped with boron. Subsequently, the polysilicon is etched into a predetermined shape and an oscillatory gate 16, i.e., a planar beam, is formed. Finally, a second sacrifice oxide is deposited on the first sacrifice oxide.